December 1969

RESEARCH AND DEVELOPMENT

OF

HIGH SPEED PROCESSOR ARRAYS

Prepared by
Philco-Ford Corporation
Microelectronics Division
Blue Bell, Pennsylvania 19422

For
Massachusetts Institute of Technology
Lincoln Laboratory

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ABSTRACT

This report describes program progress for the first four
interim periods of a research and development program directed
toward the development of high density, high performance, complex
digital arrays and their application in system feasibility
studies of a high speed Central Processor.

An important task of this program was to establish subnano-
second-minimum power ECL microcircuit designs which could be used
as effective building blocks for the Processor Arrays. This task
required the design, fabrication and evaluation of an array test
chip containing different microcircuit designs. The task was
accomplished; specific small geometry gate and reference bias
microcircuits (gate power dissipation was nominally 15 mW, inclu-
ding complementary outputs) were selected and utilized in the
design of an 80-gate Processor Master Array Chip.

Functioning high speed 256-bit Read Only Memory Arrays were
successfully fabricated. A flexible technique for programming
these ROM's at the chip level was developed and demonstrated.

Yield improvement studies were conducted. This effort
included an investigation of the applicability of the CDI process
to high speed ECL. It also included the design and evaluation of

a complex Multilevel Process Test Chip for characterizing and monitoring multilevel interconnection processes and structures.

Techniques for multichip assembly of high speed LSI chips were investigated. In particular, the fundamental processes for solder reflow face-down bonding and aluminum beam lead technology were established.

All photomasks employed during the program were designed at MIT Lincoln Laboratory using computer aid.

Accepted for the Air Force
Franklin C. Hudson
Chief, Lincoln Laboratory Office

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

I - INTRODUCTION

1.1 PROGRAM OBJECTIVE

The objective of this program is the continued development of high density, high performance, complex digital arrays and their application in high speed system feasibility studies. The study vehicle is a high speed Central Processor.

1.2 SCOPE OF REPORT

This report summarizes the progress made during the first four interims of a research and development program conducted by Philco-Ford under a subcontract with MIT Lincoln Laboratory.

1.3 AREAS OF INVESTIGATION

During this program, Philco-Ford has directed efforts toward refining and extending device, microcircuit, and LSI technologies which can be applied in complex high speed data processing systems. These refined technologies were applied in the design and fabrication of a number of high speed multilevel arrays as part of a program to implement LSI in feasibility studies of a high speed Central Processor.

One of the tasks of the program was to establish high speed ECL microcircuit designs which could be used as effective building blocks for the Processor Arrays. The achievement

of subnanosecond propagation delays per stage at the lowest possible power dissipation was a prime goal of this task.

Another important program task was the investigation of methods for improving fabrication yields of the microcircuit and multilevel interconnection processes. This investigation included a study of the effects on yield of a new simplified microcircuit process, the Collector Diffused Isolation (CDI) process, which was adopted for use in high speed ECL.

Two- and three-level arrays, including a 256-bit Read Only Memory and an 80-gate Processor Master Array, were designed, fabricated, and evaluated.

Program efforts also included continued investigation of multichip assembly techniques which are compatible with high speed systems. Included in this effort was a study of face-down bonding and beam lead technologies.

The layout designs for all microcircuits, multilevel arrays, and test vehicles employed in this program represent a cooperative effort between MIT Lincoln Laboratory and Philco-Ford, with final layout design being implemented by MIT Lincoln Laboratory using computer aid. The computer program also produces data tapes from which the photomasks were generated. Photomasks were produced using commercial pattern generator and photorepeater equipment.

II - PROGRAM DEVELOPMENTS

2.1 SELECTION OF BASIC GATE AND REFERENCE BIAS MICROCIRCUITS
     FOR PROCESSOR ARRAYS

The first task of this program was to select the basic microcircuit gate which would be used as a building block for the Processor Arrays. Because ECL was the selected logic form, it was also necessary to select an appropriate reference bias circuit.

The procedure for selection of the basic microcircuit gate and reference circuits was:

1. Selection of a range of circuit operation wherein the expected performance (in terms of speed and power) of a well-designed high speed ECL microcircuit gate was applicable for the high speed Processor. Subnanosecond speeds at minimum power were prime objective-performance characteristics.

2. Design of an evaluation test chip which contained microcircuit designs that were designed to be in the desired performance range.

3. Fabrication of the test chip and selection of gate and reference circuit designs for the Processor Arrays, based on evaluations of the test chip.

The circuit designs shown in Figure 1 were constructed onto a microcircuit test chip referred to as the SMX14. They represent a range of power dissipation which is considered acceptable for LSI application, yet over which subnanosecond operation per gate could have been expected when our high performance technology was applied. In Design #1, the current switch dissipates 10 mW, each emitter follower dissipates 10 mW and the reference circuit dissipates 20 mW, nominally. In Design #2, the current switch dissipates 5 mW, each emitter follower dissipates 5 mW and the reference circuit dissipates 10 mW, nominally.

Figure 2 illustrates the SMX14, a 100 x 100 mils^2 chip which contains, in addition to the complete microcircuits, a variety of test transistors and resistors, sheet resistance test patterns, and a via test vehicle having ten series-connected vias. Figures 3 and 4 are high magnification photomicrographs of the two gate and reference bias circuit designs.

The SMX14 test chip actually contains groups of each of the gate types, interconnected through two levels of metal in a manner that allows measurement of the basic gate speed in an array environment. Figure 5 is a schematic diagram of the interconnection scheme. After measuring $\tau_{pd(chain)}$ and $\tau_{pd(ref)}$, the average propagation delay time, τ_{pd}, of a single
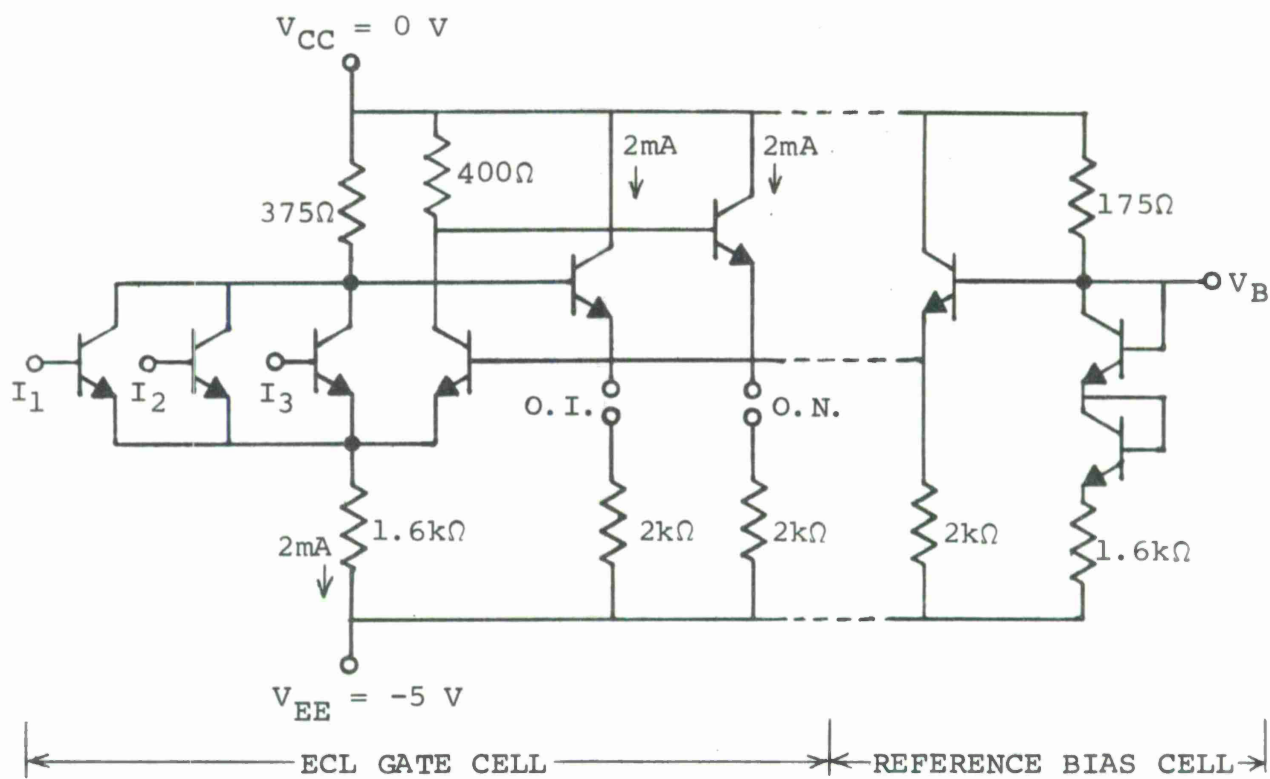
a. Design #1.
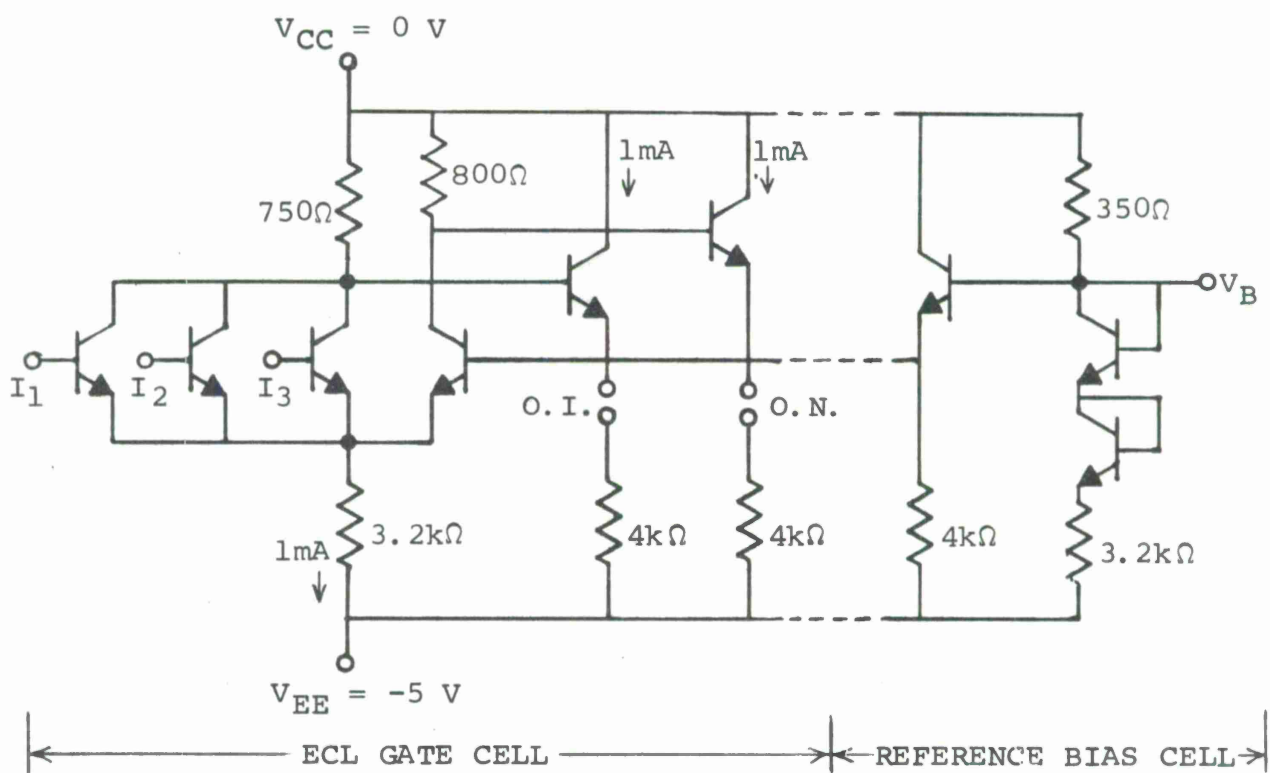
b. Design #2.

Figure 1. Schematic diagrams of high-speed ECL Gate Cells and Reference Bias Cells.

-5-

TEST
TRANSISTORS

DESIGN #1
TEST CHAIN:
7 GATES AND
1 REFERENCE
BIAS CELL

TEST PATTERN
FOR BASE
SHEET
RESISTANCE

DESIGN #2
TEST CHAIN:
7 GATES AND
1 REFERENCE
BIAS CELL

VIA TEST CHAIN   TEST RESISTORS
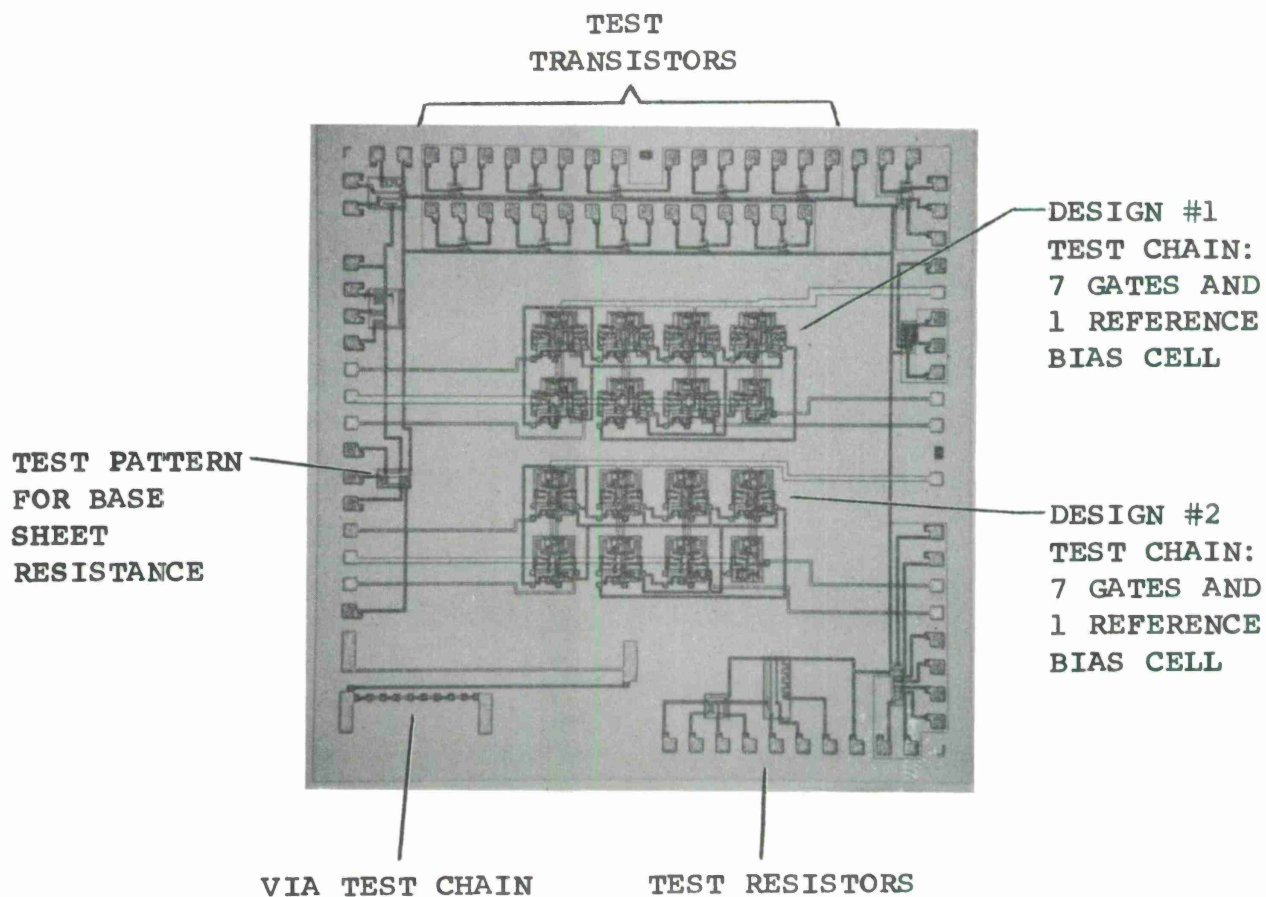
Figure 2.   Photomicrograph of SMX14 Microcircuit Test Chip.
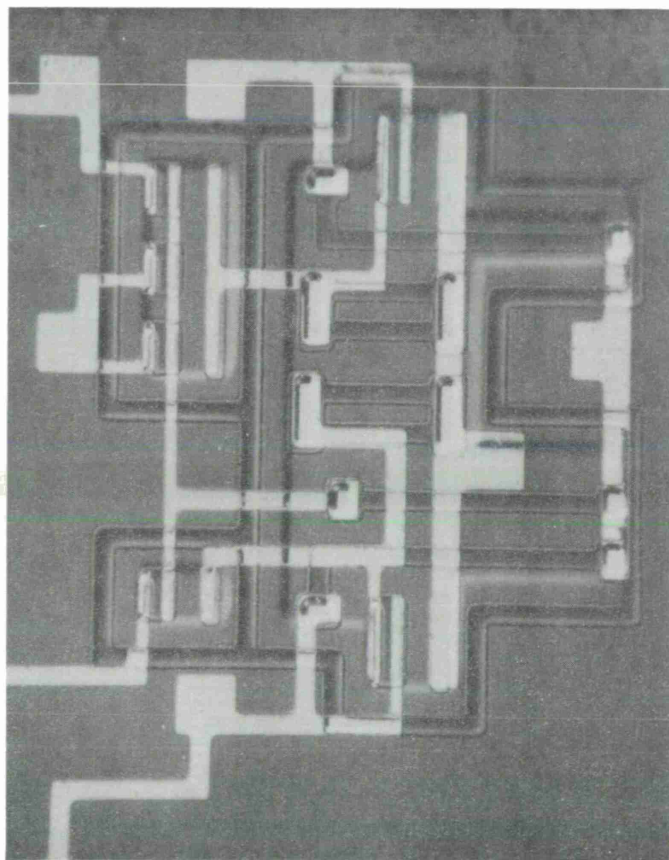
a. Gate.
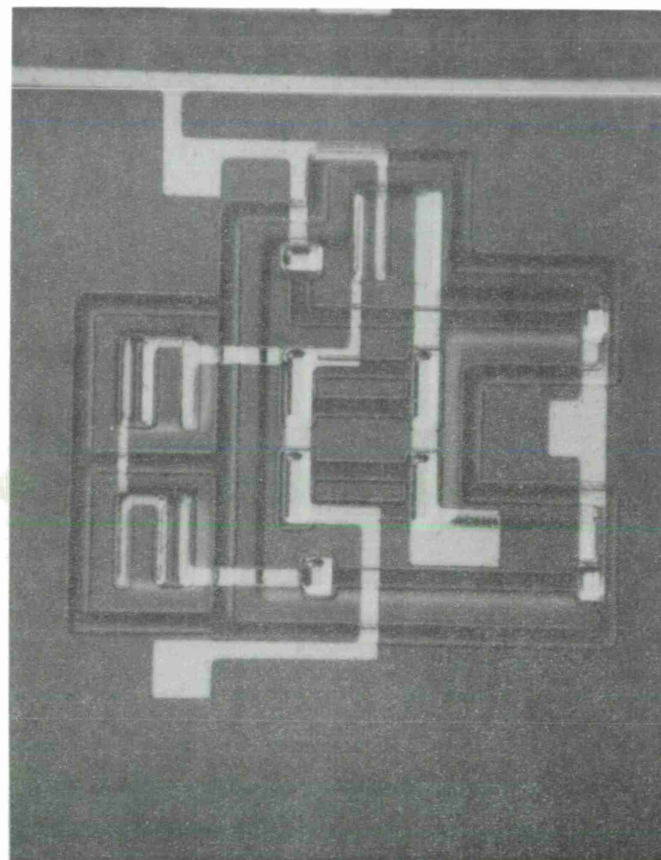
b. Reference circuit.

Figure 3.   Photomicrographs of Design No. 1 Microcircuits.
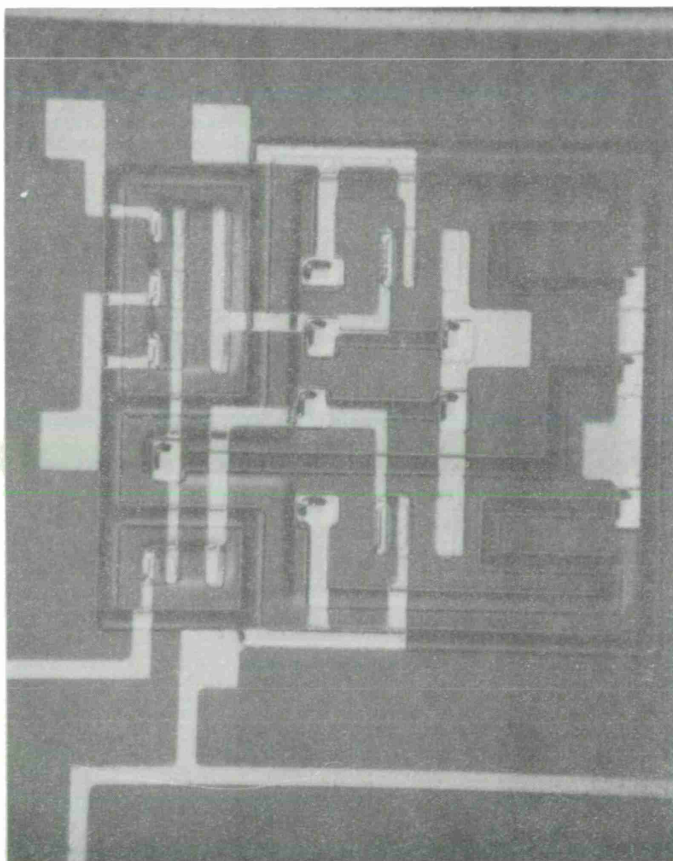
a. Gate.
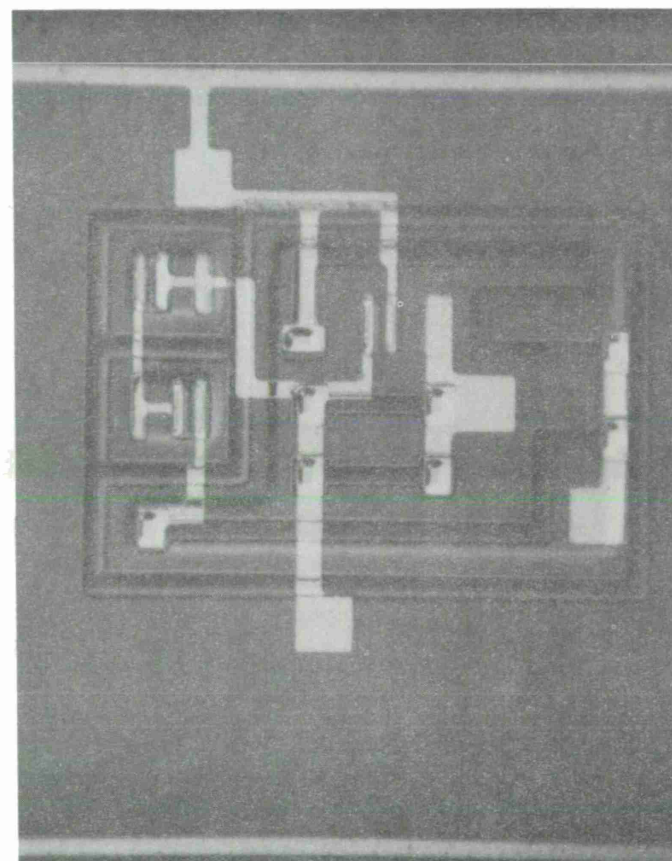
b. Reference circuit.

Figure 4. Photomicrographs of Design No. 2 Microcircuits.

NONINVERTED
(REF)

INPUT

NONINVERTED
(CHAIN)
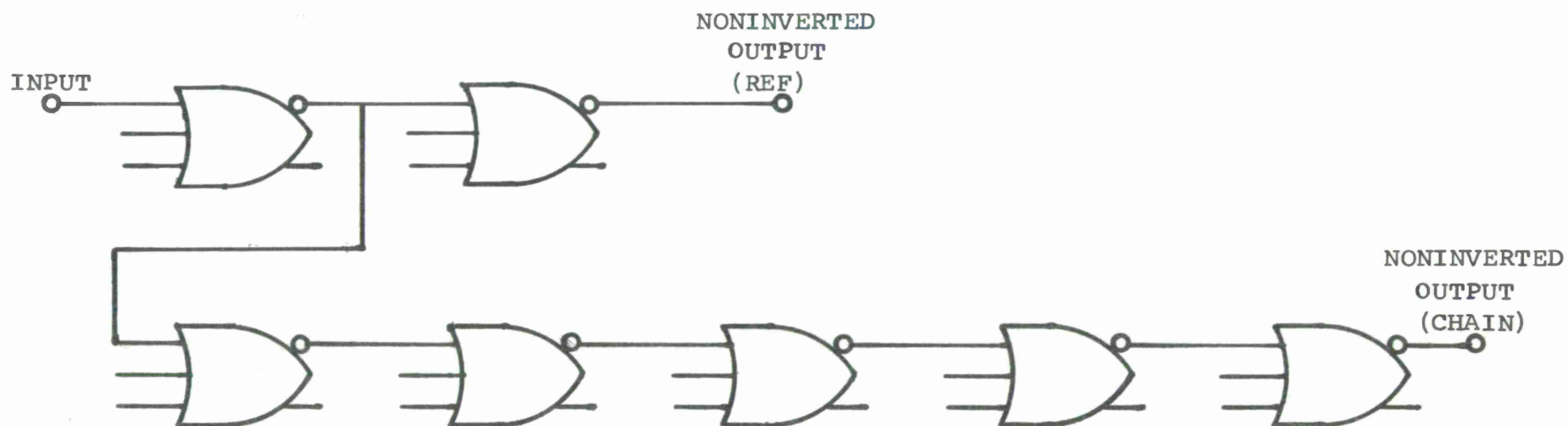
NOTE: ALL UNUSED INPUTS ARE BIASED "OFF".

Figure 5.   Schematic diagram illustrating the technique employed
to measure propagation delay time on SMX14 ECL Gates.

gate, unaffected by the test apparatus, is obtained using the

expression
$$\tau_{pd} = \frac{\tau_{pd(chain)} - \tau_{pd(ref)}}{4}$$

where $\tau_{pd(chain)}$ is the propagation delay through the chain of
six gates and $\tau_{pd(ref)}$ is the propagation delay through the
input and output stages only.

In addition to fabricating SMX14 chips with the original
design nominal resistor sheet resistance of 100 $\Omega/\square$, SMX14 chips
with 200 $\Omega/\square$ nominal resistor sheet resistance were fabricated
so that additional data could be obtained concerning speed-
power trade-offs. Speed-power data for both gate designs for
the nominal 100 $\Omega/\square$ and 200 $\Omega/\square$ chips are listed in Table I.
Each of the emitter followers in the gates was designed to
dissipate the same power as the current switch for the low
fanout condition present on the SMX14 chip. Consequently, total
gate power is three times the power dissipated in the current
switch. Inasmuch as resistors were fabricated 20% above design
value, power dissipations listed in Table I are approximately
20% lower than design value.

Table I indicates that both versions of the 100 $\Omega/\square$ gates
meet the design goal of subnanosecond operation but that the
200 $\Omega/\square$ gates would did not exhibit subnanosecond delays at both
outputs, especially under fanout conditions greater than one.
The above conclusion is based partly on calculations since the

-10-

TABLE I

PROPAGATION DELAY - POWER DISSIPATION DATA FOR HIGH SPEED
GATE DESIGNS #1 AND #2

Nominal Sheet Resistance	GATE DESIGN (see Fig.1)	Current Switch Power (mW)	Total Gate Power* (mW)	Measured τ_{pd} (Noninverted) Output (ns)	Calculated τ_{pd} (Noninverted) Output (ns)	Calculated τ_{pd} (Inverted) Output (ns)
100 $\Omega/\square$	#1	8.2	24.6	0.52	0.47	0.73
	#2	4.2	12.6	0.61	0.64	0.98
200 $\Omega/\square$	#1	4.1	12.3	0.83	0.82	1.33
	#2	2.0	6.0	1.07	1.17	1.86

*
Includes power in current switch and the complementary emitter followers.

-11-

inverted output of the gates cannot be tested on the SMX14.
However, since the calculated and measured delays agree well for
the noninverted output, the calculation of delay for the inverted
output is realistic. The calculations were made at Lincoln
Laboratory.

The transistors used in Gate Designs No. 1 and No. 2 are
shown in Figures 6b and 6a, respectively. Typical f_T vs. I_E
curves for these devices are shown in Figures 7a and 7b. The
emitter follower transistors were designed to conduct 4 mA and
2 mA (Designs No. 1 and No. 2, respectively) under maximum fanout
conditions. The main difference in propagation delay between
Designs No. 1, 200 $\Omega/\square$, and Design No. 2, 100 $\Omega/\square$, both of which
dissipate approximately 12 mW total, can be explained in terms
of the difference in transistor sizes in the respective designs.
The principal contribution to the delay of these gates comes from
the collector time constant of the gate and reference transistors.
For example, the collector time constant for the reference
transistor (noninverted output) is given by:

$$\tau_C = R_C \ (C_{ISOL} + C_{RC} + C_{EF} + C_C)$$

where

C_{ISOL} = Isolation capacitance of the reference transistor
island.

C_{RC} = Parasitic capacitance of the load resistor

-12-

INPUT AND
REFERENCE
TRANSISTOR
(EMITTER LENGTH =
0.3 MIL)

EMITTER FOLLOWER
OUTPUT TRANSISTOR
(EMITTER LENGTH =
0.6 MIL)

←——— BASE CONTACT ———→

←——————EMITTER————→

←—— COLLECTOR CONTACT ——→
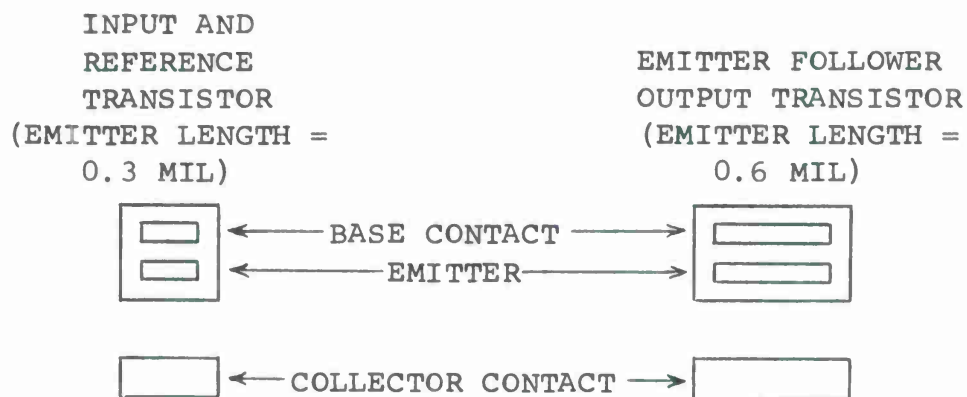
a.   Transistors employed in Gate Design #2.

SCALE: →| |← = 0.1 MIL

INPUT AND
REFERENCE
TRANSISTOR
(EMITTER LENGTH =
0.5 MIL)

EMITTER FOLLOWER
OUTPUT TRANSISTOR
(EMITTER LENGTH =
1.0 MIL)

←——— BASE CONTACT ——→

←—————— EMITTER ——→

←—— COLLECTOR CONTACT →
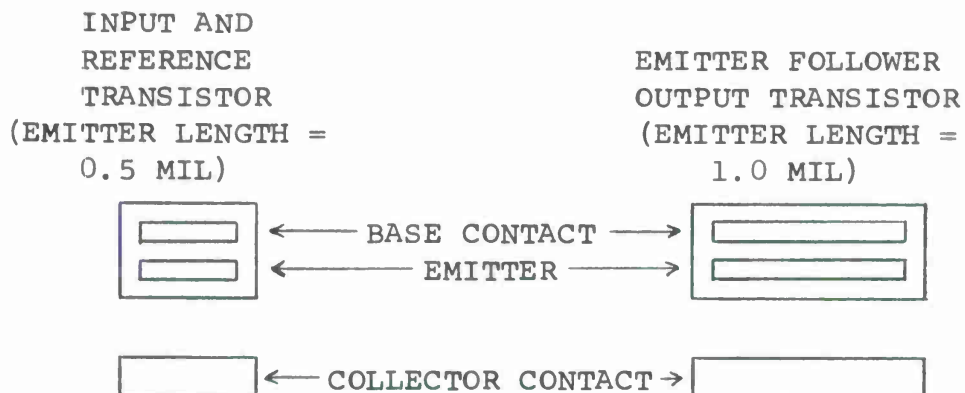
b.   Transistors employed in Gate Design #1.

Figure 6.   Diagram of small geometry, high speed transistors
            employed in SMX14 Gate Cells.
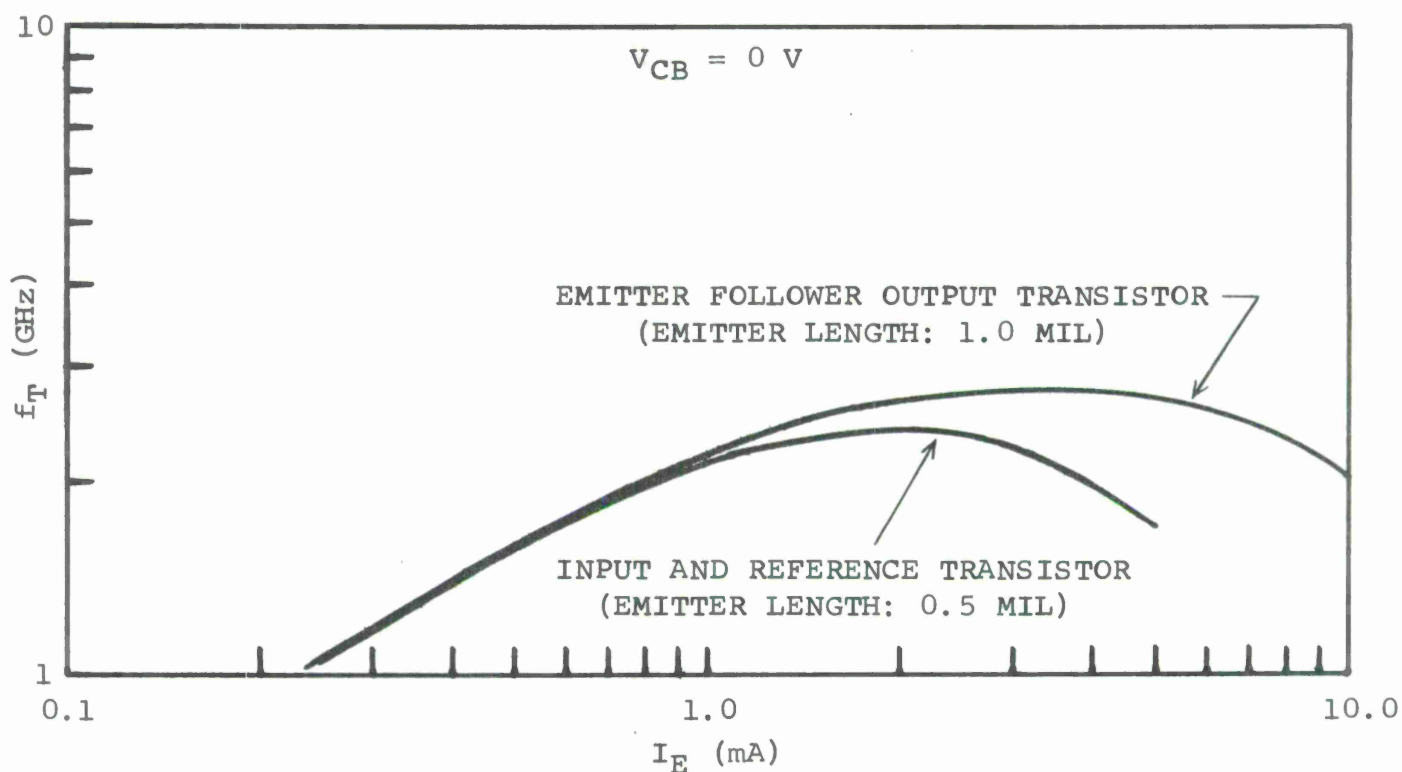
Figure 7a. f_T versus I_E for transistors of Gate Design #1.
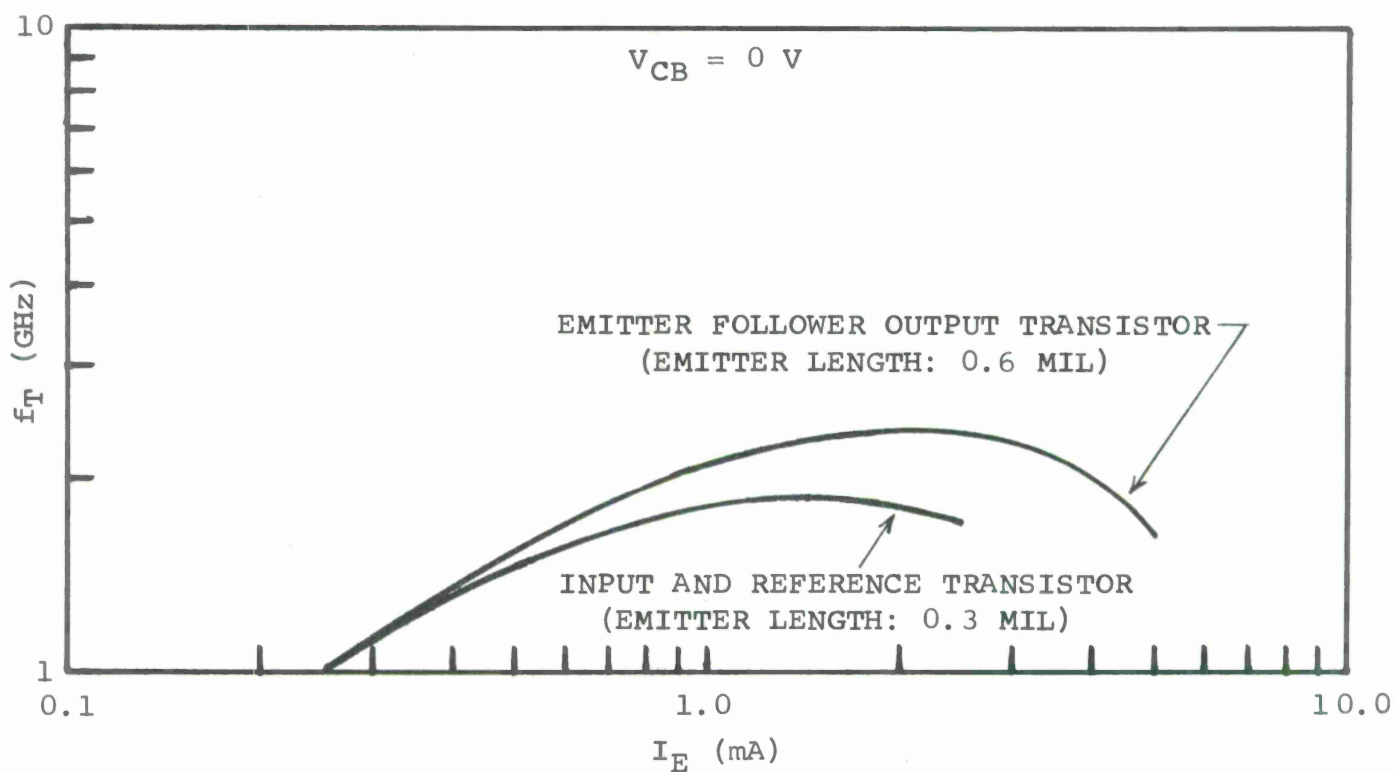
Figure 7b. f_T versus I_E for transistors of Gate Design #2.

C_{EF} = Input capacitance of the emitter follower.

C_C = Capacitance looking back into the reference transistor.

Design No. 1 employs larger transistors, and consequently, C_{ISOL}, C_{EF}, and C_C are all higher than in Design No. 2. The net result is a 25 to 30% increase in τ_{pd}.

Based on the data shown in Table I, Design No. 2, 100 $\Omega/\square$, was selected for tentative use in the Processor Arrays. Later in the program, Design No. 2 was incorporated into an 80-gate array design referred to as the Processor Master Array, described in subsection 2.3.

2.2 READ ONLY MEMORY ARRAY

Another program task was the design and fabrication of a high speed programmable 256-bit Read Only Memory (ROM) Array. Shown schematically in Figure 8, the ROM consists of an array of 256 high speed transistors interconnected through two levels of metal to form a programmable matrix of 16 words, with 16 bits per word. This ROM chip, designated the SMX15, is a refined version of the ROM developed during the previous program.[*] The refinements include:

1. Transistors having a larger drive capability,

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[*]"R&D of the Technologies Required to Design and Fabricate Ultrahigh-Speed Computer Systems," Final Report dated January 1969 covering the period July 1, 1967 to June 30, 1968, prepared by Philco-Ford Corporation, Microelectronics Division, for MIT Lincoln Laboratory under Purchase Order No. BB-114, Prime Contract No. AF19(628)5167.
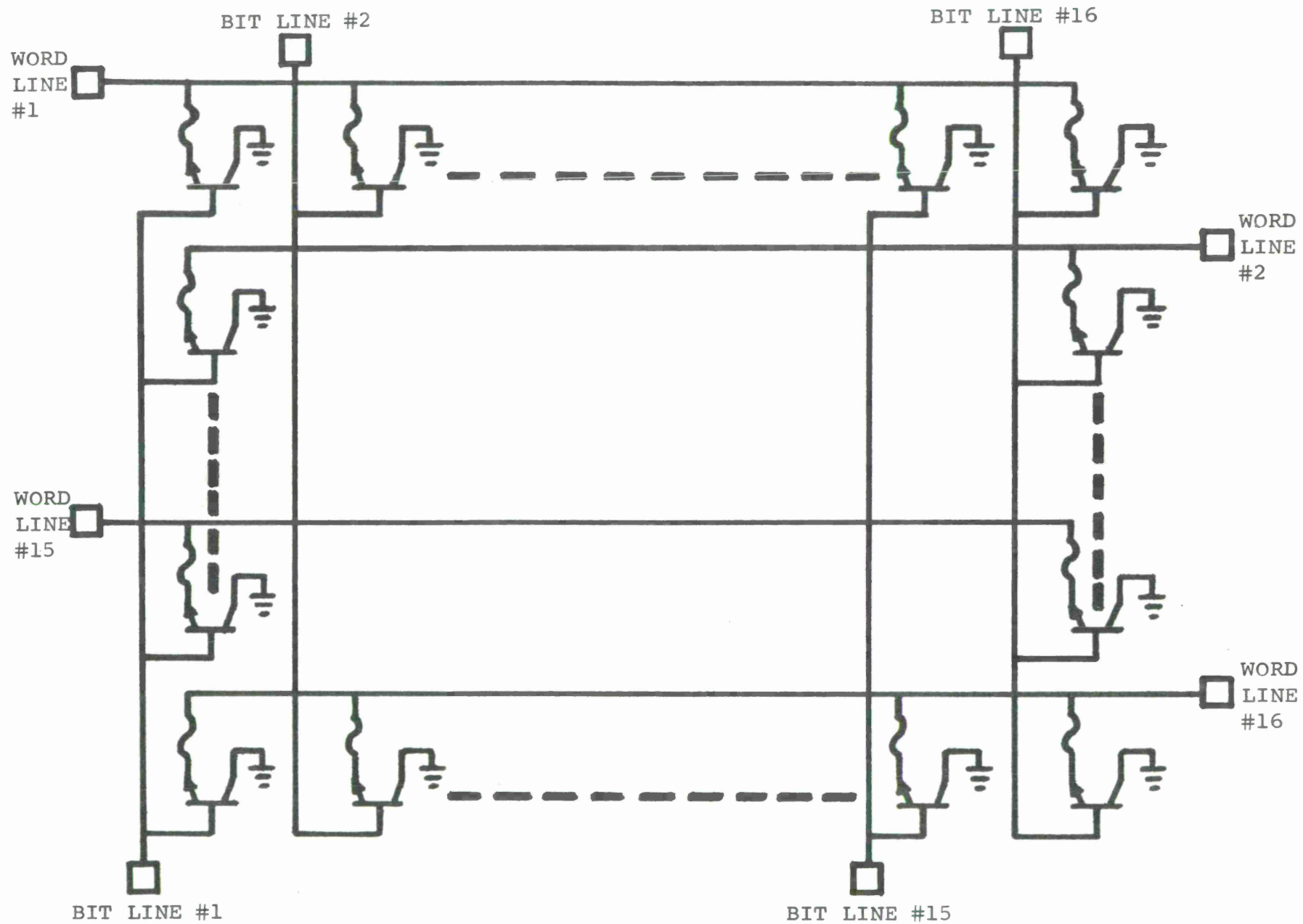
Figure 8. Schematic diagram of Read Only Memory Array.

2. Programming options provided in the emitter-conductor lines rather than in the base-conductor lines, and

3. Fine-line fuse links provided in the second level of metal so that programming of the ROM can be attempted at the chip level.

Several lots of Read Only Memory Arrays were fabricated during this program. Figure 9 is a photomicrograph of the ROM Array. Chip size is 66 x 66 mils^2. The best yield per wafer obtained at die sort was 8.4%. Statistical calculations indicate that 99% transistor yields were achieved on this wafer.

Programming of the high speed SMX15 ROM can easily be accomplished at the wafer level through use of a custom designed photomask at virtually any step in the fabrication process. Quickest turn-around time using this approach is obtained by fabricating and storing wafers in nearly completed form and performing the customizing at either the insulator cut or top-level-metal etch operations. However, during the early stages of the Processor study program, it was anticipated that relatively small numbers of a large quantity of customized ROM chips would be required. In this case, the maximum flexibility and lowest turn-around time is achieved if the ROM's are programmable at the chip level. Consequently, a mechano-chemical technique was
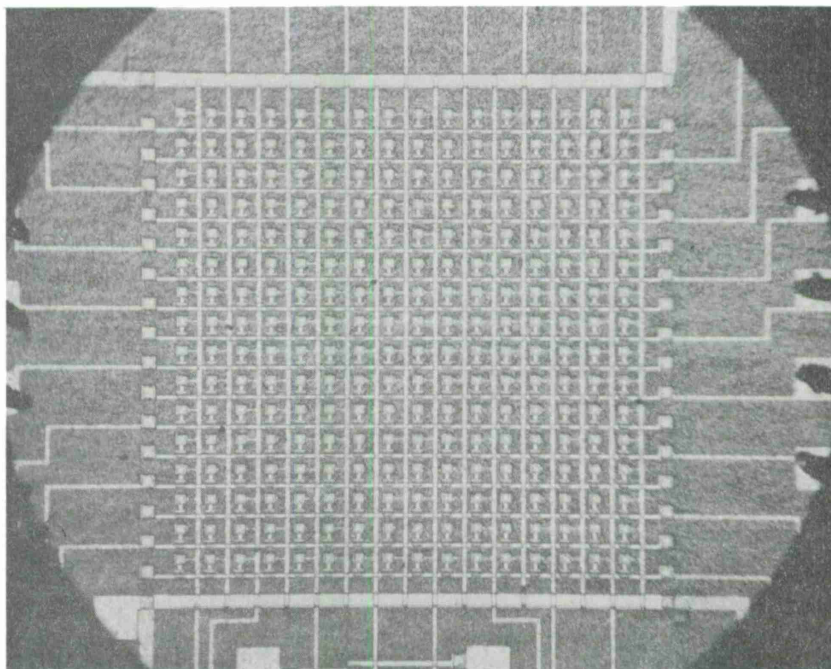
Figure 9. Photomicrograph of 256-Bit Read Only Memory Array.

developed for programming the ROM top-level metal after chips

have been fully tested. This programming technique is applicable

before or after the wafer is scribed or even after chips have

been bonded in a package. Figure 10 shows a high-magnification

photomicrograph of a portion of a ROM chip which was programmed, after

the chip was bonded in a package, by removing sections of the

top-level metal at selected bit sites.

Sample programmed ROM's were delivered to Lincoln

Laboratory.

2.3 PROCESSOR MASTER ARRAY (SMX17)

Subsection 2.1 describes the basic gate and bias reference

cells which were selected for use in the initial high speed LSI

arrays to be used in the Processor study. During the fourth

interim of the program, final design was completed for the

first Processor Array, the Processor Master Array. This array,

which contains a matrix of 80 three-input ECL gates and 16

reference bias cells and has a chip size of 120 x 130 mils^2,

can be interconnected with three levels of custom metallization

to form several required system subfunctions. Custom metallization

masks for generating a 4-bit Full Adder (SMX17A) were designed

with the Master Array late in the fourth interim--too late,

however, to obtain fabricated arrays before the end of this

interim. The Adder chip is planned to be one of the first arrays

to be developed during an extension program which has been

proposed to Lincoln Laboratory.

0.3 MIL
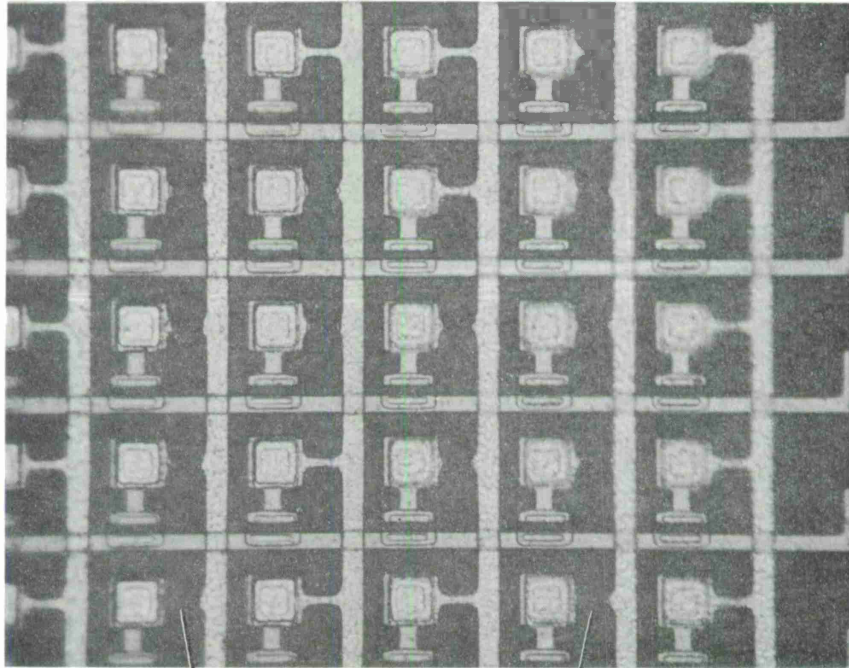
TOP LEVEL METAL REMOVED AT SELECTED BIT SITES

Figure 10. Photomicrograph of a programmed ROM.

The Master Array also offers an excellent vehicle for studying the performance of the Processor basic gate under a variety of ON-chip array loading conditions. Custom metallization masks for fabricating a Loading Test Chip were designed and are described in subsection 2.4.

During use of the Master Array photomasks, several minor corrections were made in the mask set. One lot of Master Array Wafers was completed (up to first-level metal) with corrected masks. This lot will be completed as Loading Test Chips.

Figure 11 illustrates the Processor Master Array chip after first level metal. In addition to the microcircuit cell matrix, the chip contains test transistors and resistors typical of those used in the microcircuits, a multi-emitter test transistor for characterizing transistor yield and provisions for a via test chain when the metallization is completed.

2.4 PROCESSOR LOADING TEST CHIP (SMX17L)

The basic gate configuration chosen during the second interim for use in Processor Arrays was characterized for ON-chip delays under fanin and fanout conditions of 1 on the SMX14 Test Chip. The Loading Test Chip was designed to characterize performance of the basic gate under various system simulating intra-chip loading conditions. The various gate test configurations present on the Loading Test Chip are as follows:

-21-
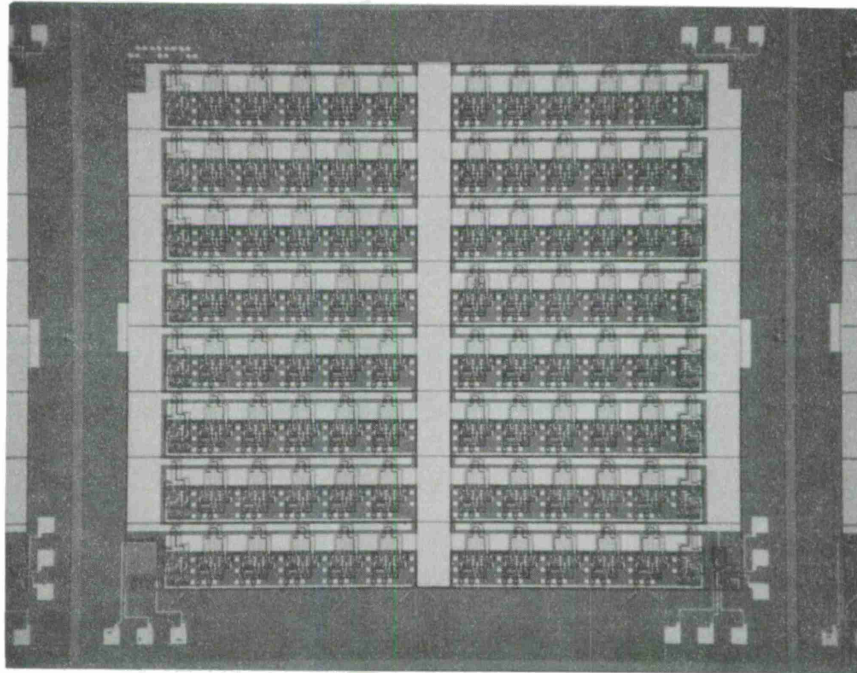
Figure 11.   Photomicrograph of Processor Master Array Chip.

1. Single gate.

2. Flip-Flop (interconnection of 2 gates).

3. Propagation delay chain wherein test gates are operated with fanout and fanin of 1, inverting outputs doing the driving.

4. Propagation delay chain wherein test gates are operated with fanout and fanin of 1, noninverting outputs doing the driving.

5. Propagation delay chain wherein test gates are operated with fanout of 7 and fanin of 1, noninverting outputs doing the driving.

6. Propagation delay chain wherein test gates are operated with fanout of 1 and fanin of 7, noninverting outputs doing the driving.

The propagation delay chains are very similar to that of Figure 5, differing only in that delay is averaged over 7 gates in the Loading Test Chip whereas 4 gate delays are averaged on the SMX14.

In addition to the listed gate configurations, the Loading Test Chip contains the same transistor, resistor, and via test devices which are on the Master Array. Figure 12 is a photomicrograph of a Loading Test Chip.

One wafer of Loading Test Chips was completed by the end of the fourth interim. Evaluations of this wafer and accompanying
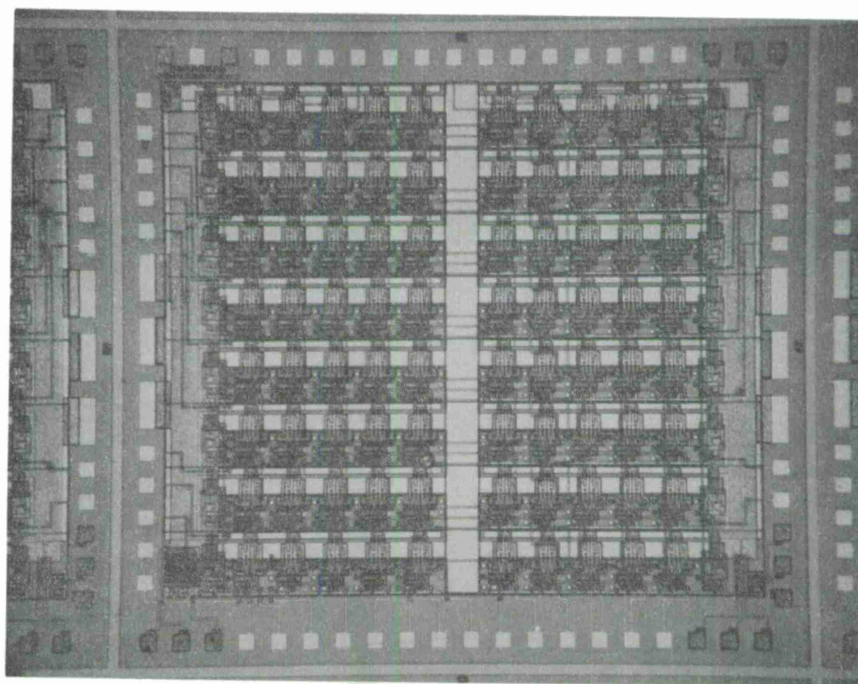
Figure 12.   Photomicrograph of the Loading Test Chip.

test wafers indicated that modifications are required in our three-level metal process. The problem is discussed in subsection 2.6. A number of remedial approaches are being evaluated; it is expected that an improved three-level process will be developed by the starting date of the proposed extension program at which time additional wafers of Loading Test Chip will be fabricated.

2.5 MICROCIRCUIT YIELD STUDIES

Throughout this program, studies were directed toward the improvement of yields in high performance microcircuit structures. These studies were focused not only on the standard high performance process which we have developed and refined over the past few years but also included an investigation of the merits of a new process, the Collector Diffused Isolation (CDI) process, as adapted to high speed ECL.

2.5.1 Standard High-Performance Process

The yields of high performance microcircuits are affected by numerous factors relating to the design and fabrication of the microcircuits. These factors include effective design rules and proper control of such essential processes as silicon growth and wafer preparation, thin layer epitaxy, oxidation, shallow diffusion, fine line photoengraving and metallization. During

the past few years, we have evolved an effective combination of design rules and processing for the reproducible generation of subnanosecond microcircuits and have successfully continued these efforts on this program.

During this program, refinements were made in our standard small-geometry, high-performance microcircuit fabrication process which have virtually eliminated the incidence of transistor emitter-base shorts. Yield analyses that were made on a number of lots of SMX14 and ROM wafers have substantiated that transistor yield loss due to emitter-base diode degradation is consistently less than 1%.

By minimizing emitter-base defects and by adding refinements to our photoengraving and wafer processing, micro-circuit transistor yields have been maintained consistently in the 96% to 99% range. This capability has enabled the success-ful fabrication of a 256-transistor Read Only Memory at yields as high as 8.4% (subsection 2.2). It has also enabled the fabrica-tion of SMX14 chips containing, effectively, 16 functional gates at yields as high as 33.5%. The yield of 8-gate arrays (i.e., an SMX14 chip wherein one gate chain was functional) ran as high as 50%. Figure 13 is a yield map showing the distribution of chips having 8 and 16 functional gates.
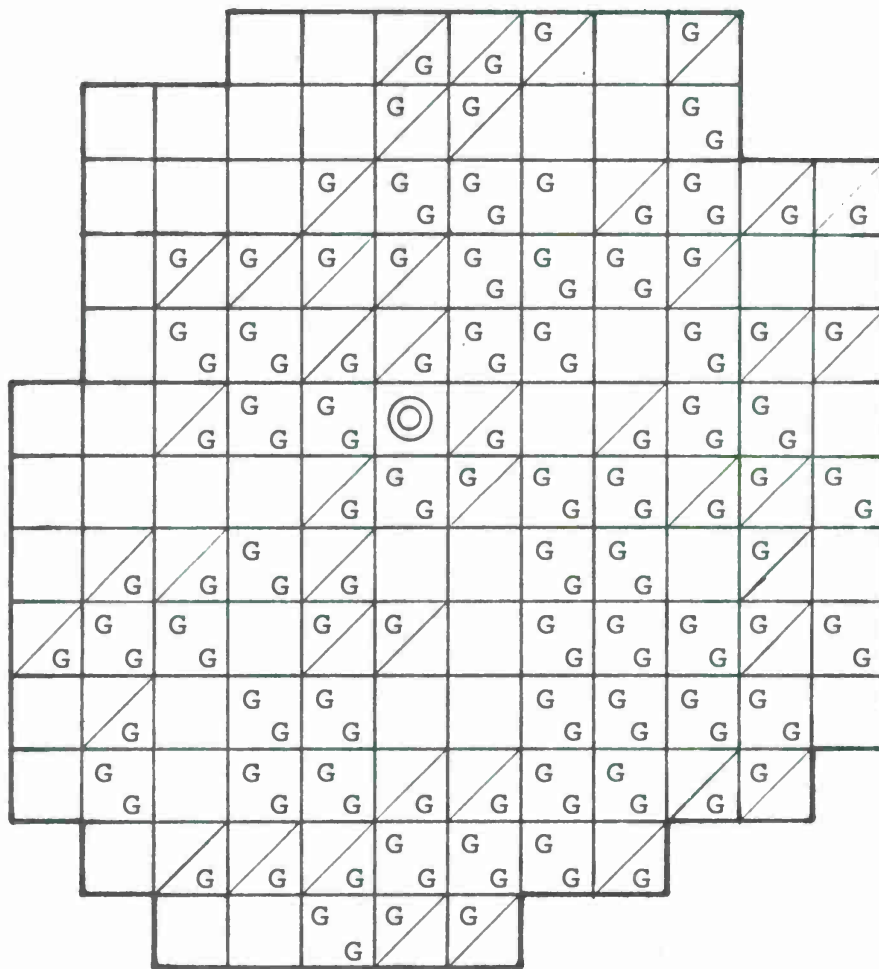
YIELDS

G / -- 8 FUNCTIONAL GATES - DESIGN #1 - 49.2%

/ G -- 8 FUNCTIONAL GATES - DESIGN #2 - 50.0%

G
 G - 16 FUNCTIONAL GATES - - - - - - - - 31.6%

Figure 13. Yield map of SMX14-9-2D illustrating the distribution
of chips containing effectively eight and sixteen
functional gates.

The remaining 1 to 4% transistor yield loss is due to emitter-to-collector defects. We believe these emitter-to-collector defects are due to n-type pipes which, due to process-induced material defects, locally penetrate the base during the emitter diffusion. A series of experiments have led to the conclusion that there is a strong possibility that the cause of emitter-collector defects is related to the emitter-diffusion process itself. A developmental effort aimed at improving the emitter-diffusion process has been initiated.

2.5.2 Collector Diffused Isolation (CDI) Process

Microcircuit yield is inversely related to microcircuit area and to the complexity of the fabrication process. In principle, a reduction either in microcircuit area or in process complexity should give improved yield. An important task of this program was an investigation to determine whether high-performance ECL microcircuits can be made at higher yield through use of "simpler" processing sequences. The specific process developed for this purpose is a form of the Collector Diffused Isolation (CDI) Process introduced by B. Murphy et al.[1]

In order to evaluate the relative merits of the high performance CDI Process that was developed, the CDI Process was compared to the high performance Standard Process in terms of

process complexity, microcircuit performance, microcircuit component density, and laboratory yield. The comparison was made by designing, fabricating and evaluating with each process a high speed ECL microcircuit gate employing identical circuit designs and identical microcircuit transistors. Both microcircuits were fabricated for two ranges of power dissipation and speed. Both microcircuits employed small geometry (0.1 mil), shallow diffused transistors (base depth = 0.45 to 0.6 μ) with f_T values of 2 to 3 GHz.

2.5.2.1 Process Complexity

Table II compares our high speed CDI and Standard Processes. It is evident that the CDI Process is simpler, requiring three less major operations (to the point of first-level metal), two less photoengraving operations, and one less diffusion. Fundamental differences in the processes (the bracketed steps in Table II) include the following:

1. The CDI Process employs a thin p-type epitaxial layer ($\sim$1.2 μ) which becomes the transistor base and resistor regions; the Standard Process employs a thicker n-type epitaxial layer ($\sim$4 μ) into which the transistor base and resistors are subsequently diffused.

TABLE II

COMPARISON OF HIGH SPEED STANDARD AND CDI PROCESSES

STANDARD PROCESS	CDI PROCESS
● P^- SUBSTRATE OXIDATION	● P^- SUBSTRATE OXIDATION
● BURIED N^+ CUTS AND DIFFUSION	● BURIED N^+ CUTS AND DIFFUSION
● N EPI LAYER GROWTH	● P EPI LAYER GROWTH
● EPI OXIDATION	● EPI OXIDATION
● P ISOLATION CUTS AND DIFFUSION	● N^+ FEED-THROUGH CUTS AND DIFFUSION
● RESISTOR, INSERT CUTS AND DIFFUSION	
● BASE CUTS AND DIFFUSION	● BASE, RESISTOR DIFFUSION
● EMITTER, COLLECTOR CUTS AND DIFFUSION	● EMITTER, COLLECTOR CUTS AND DIFFUSION
● CONTACT CUTS	● CONTACT CUTS
● CONDUCTOR EVAPORATION AND DELINEATION	● CONDUCTOR EVAPORATION AND DELINEATION
16 Major Steps	13 Major Steps
7 Masks	5 Masks
5 Diffusions	4 Diffusions

2. In the Standard Process, three photoengraving
and three separate p diffusions are used to
form the isolation structure, resistor and
base regions, respectively. In the CDI Process,
one photoengraving operation and one n^+ diffusion
define the isolation, resistor and base regions.
An additional nonlocal p diffusion is subse-
quently performed to determine resistor and base
sheet resistance. This diffusion is performed
over the entire wafer after all oxides have been
etched off.

Although the CDI Process is simpler than the Standard
Process, the required control of the epitaxial layer growth
is much more critical. Control is important because variations
in epitaxial layer thickness become identical variations in
transistor basewidth. Since the desired transistor basewidth
is on the order of 0.1 μ, the required control of epitaxial thick-
ness is about ± 0.03 μ. For the Standard Process, epitaxial
layer thickness can vary by ± 0.3 μ without affecting transistor
parameters essentially. Figures 14 and 15 show cross sections
of transistors made using both processes.

2.5.2.2 Microcircuit Density

The ECL gate which was designed and fabricated using both
processes was the basic gate selected for use in the Processor
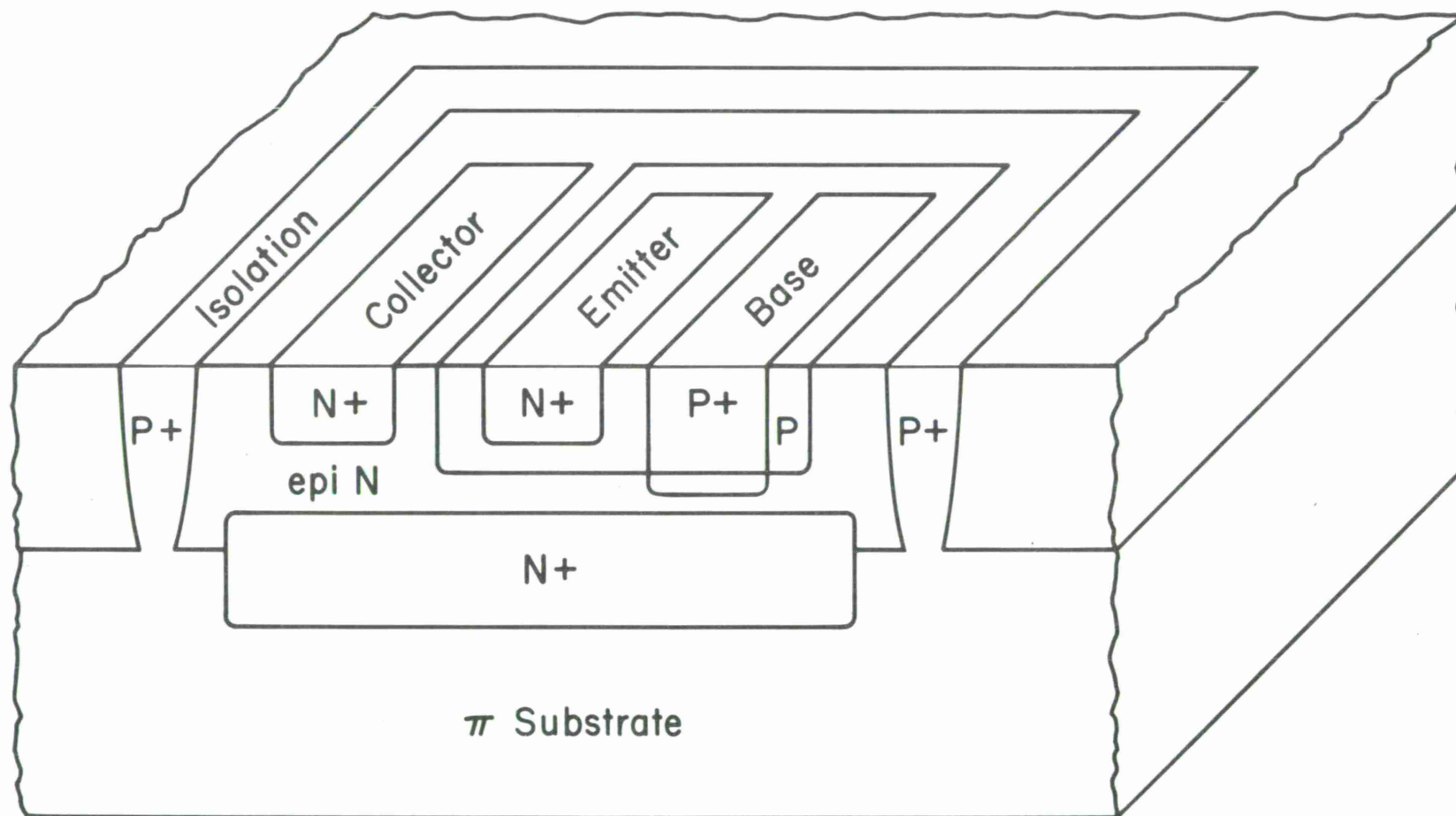
Figure 14.   Conventional Transistor.
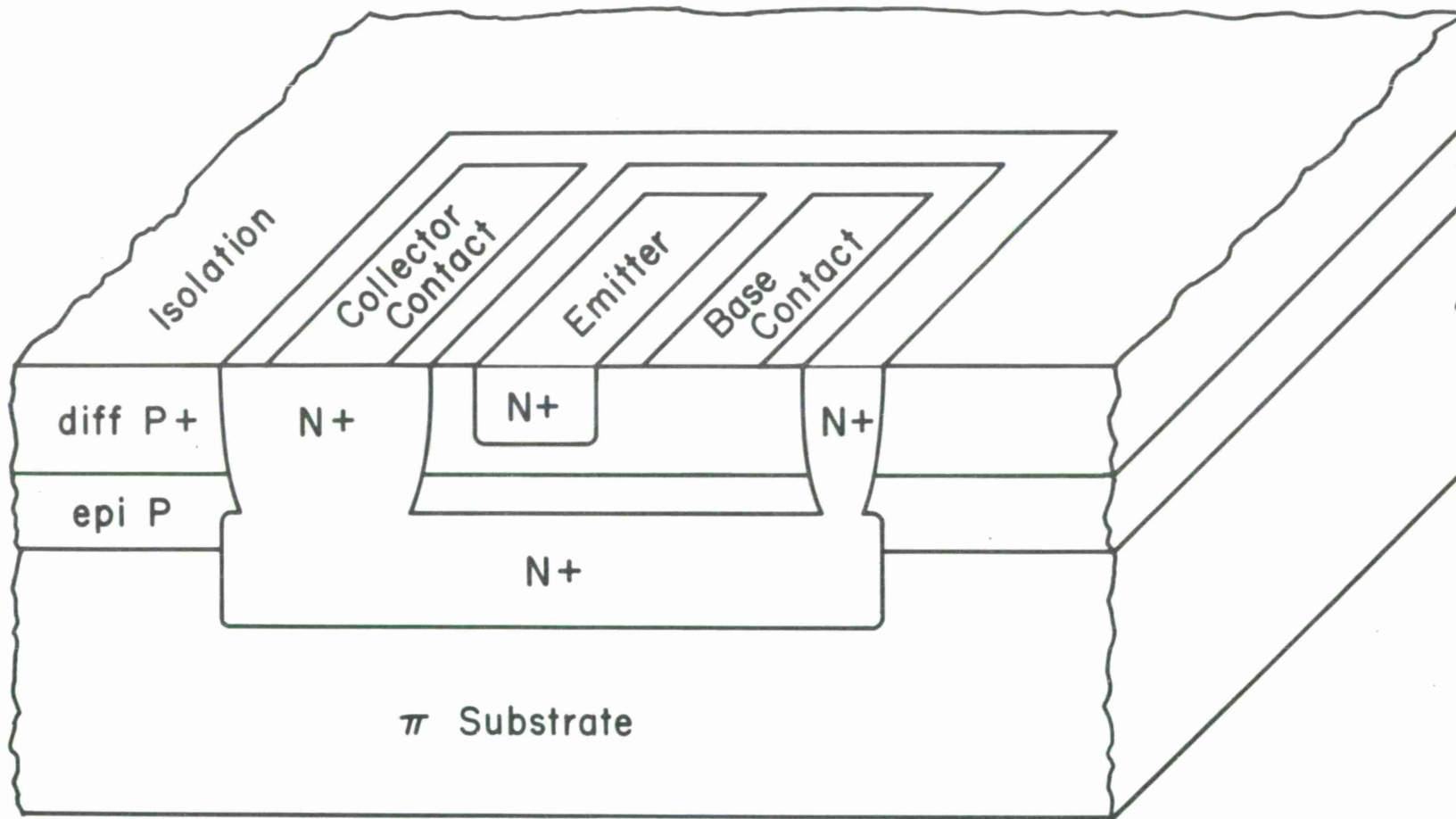
Figure 15.   CDI Transistor.

as shown in Figure 1b. After designing the ECL microcircuit gate
using CDI design rules and comparing it with an identical gate
designed with Standard Process design rules (Design #2, SMX14), it
was found that the active area of the CDI gate was only half the
area of the Standard gate (see Figure 16). Part of the area reduc-
tion results from the fact that the resistor sheet resistance in
the CDI gate is typically 400 to 800 $\Omega/\square$, whereas it is 100 to
200 $\Omega/\square$ in the Standard Process. Part of the area reduction
results from the manner in which isolation is achieved in the CDI
Process.

2.5.2.3 Microcircuit Performance

The CDI microcircuit gate was designed using a specified
resistor sheet resistance of 400 $\Omega/\square$. In order to compare
several power versions of the gate, microcircuit wafers were
fabricated with resistor sheet resistance values of 400 $\Omega/\square$ and
800 $\Omega/\square$. These gates are equivalent in power dissipation
(15 mW and 30 mW, respectively) to the 100 $\Omega/\square$ and 200 $\Omega/\square$
Standard Process versions of the #2 gate design on the SMX14
chip (see subsection 2.1). All gates were tested for propagation
delay time by using the technique illustrated in Figure 5.
Results are listed in Table III. Note that in both power versions,
the Standard gate was twice as fast as the CDI gate. In the
case of the Standard Process, the seven gates were all on one
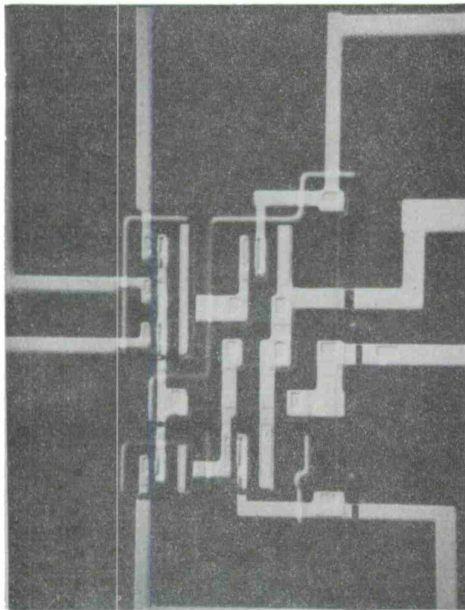
COLLECTOR DIFFUSED ISOLATION
PROCESS
(Active Area = $23\,\text{mils}^2$)
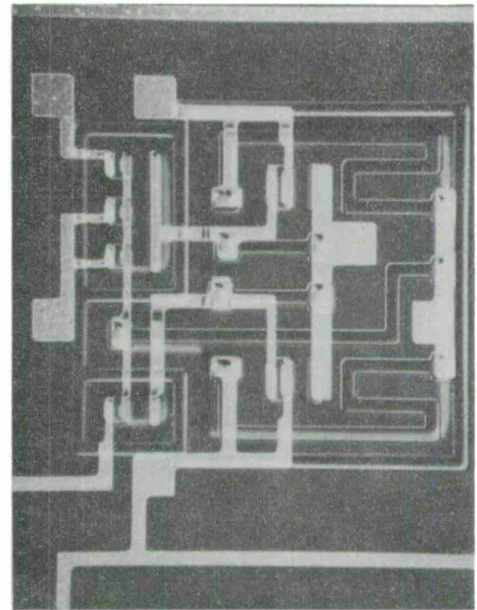
STANDARD BURIED COLLECTOR
PROCESS
(Active Area = $46\,\text{mils}^2$)

Figure 16.   Comparison of ECL Gates fabricated using High Speed
Standard and CDI Processes.

TABLE III

SUMMARY OF GATE PERFORMANCE*

Standard Process			CDI Process		
Resistor Sheet ρ ($\Omega/\square$)	Nominal** Gate Power (mW)	Average τ_p (nsec)	Resistor Sheet ρ ($\Omega/\square$)	Nominal Gate Power (mW)	Average τ_p (nsec)
100	15	0.60	400	15	1.20
200	7.5	1.07	800	7.5	2.15

* $V_{cc} = 0$, $V_{EE} = -5.2$ V; signal swing = 800 mV; noninverted output.

** Gate power includes power dissipated in both emitter followers; the power dissipated in the current switch is the same as that dissipated in each emitter follower.

chip (SMX14 chip). In the case of the CDI gate, seven discrete chips were interconnected in a single package. A 14-lead metal bottom flat package was used in both cases.

The factor-of-two differences in speed between the two processes can be attributed to the higher r_b' and collector base capacitance inherent in the CDI transistor and the higher parasitic capacitances inherent to the CDI resistor and isolation structures. Figures 17 and 18 compare r_b' and f_T for transistors made with each process. Table IV compares d-c transistor parameters. Two interesting properties of the CDI transistor which do not relate to the observed propagation delay of the CDI can be seen from Figure 18 and Table IV:

      a.   Figure 18 shows that the CDI transistor, because of its lower collector series resistance, has a much higher current handling capability.

      b.   Table IV shows that voltage breakdowns in the CDI never exceed 7.0 V because all p-n junctions in the structure have a heavily doped n-type region.

2.5.2.4 Microcircuit Yield

In order to determine relative yields for the two processes, die sort data for the CDI single gate were compared
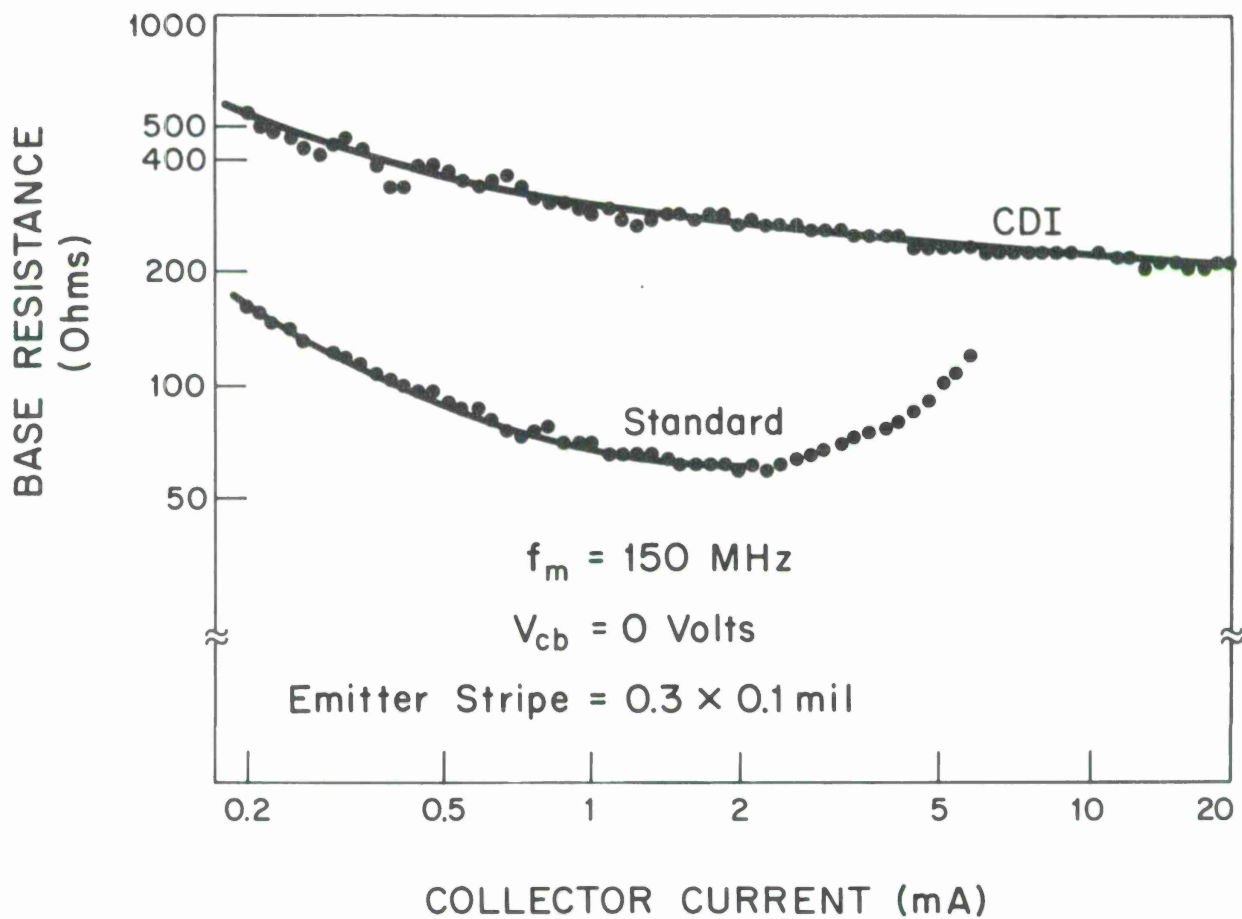
Figure 17. Comparison of r_b' for Standard and CDI Transistor.
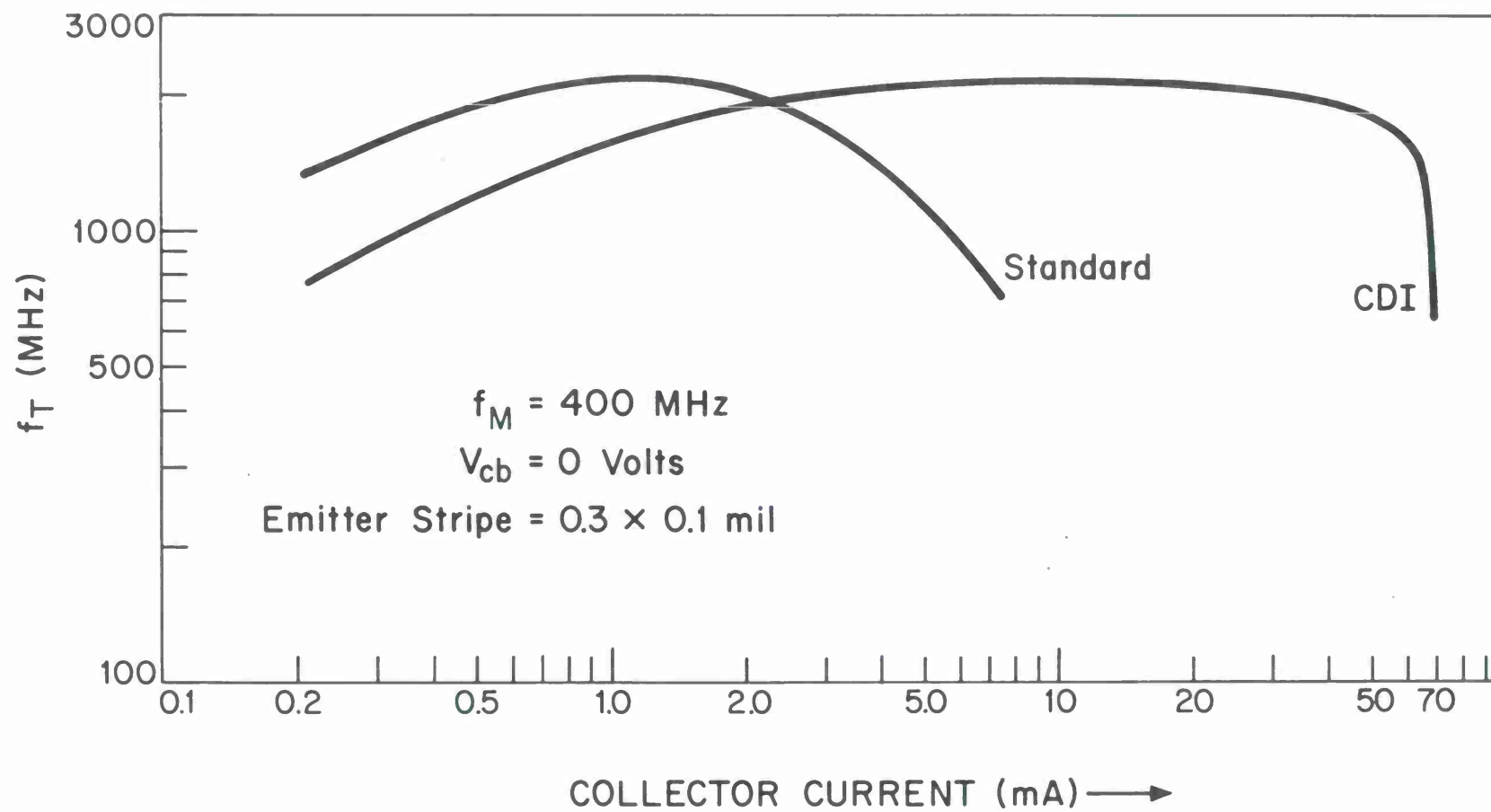
Figure 18. Comparison of Standard and CDI Transistor gain-bandwidth product.

TABLE IV

TRANSISTOR PARAMETERS

	Standard Process	CDI Process
β_N(1 mA)	72	60
BV_{CBO}(10 μA)	17.2 V	7.0 V
BV_{CES}(10 μA)	10.8 V	4.7 V
BV_{CEO}(10 μA)	8.3 V	2.8 V
BV_{EBO}(10 μA)	6.2 V	5.7 V

with die sort data obtained for Standard Process single gates fabricated approximately a year ago. Yields were comparable for the two processes, being in the range of 45 to 50%. Figure 19 shows die sort maps for two typical wafers. This data shows that the two processes give equivalent yields when compared at similar levels of development.

Examination of the CDI map reveals a clustering of good and bad areas. The failure mode of the bad areas was predominantly indicative of insufficient control of the critical p-type epitaxial layer. Gate yield in the good central area was about 70%. If we assume that epitaxial thickness variation is eliminated as a problem, the data indicate that a 70% yield of single gates can be expected. This is comparable with present Standard Process gate yields (70 to 90%) which are calculated from multiple gate data obtained on SMX14 wafers. Once again, it appears that the two processes give similar yields when compared at similar levels of development. Theoretically, CDI gate yields should ultimately be higher because of the simpler processing sequence.

In conclusion, our investigation has shown that when comparing the high speed CDI and Standard Processes, the CDI Process: (1) is the simpler process, (2) allows a two-to-one increase in component density, (3) can be expected to give

CDI PROCESS
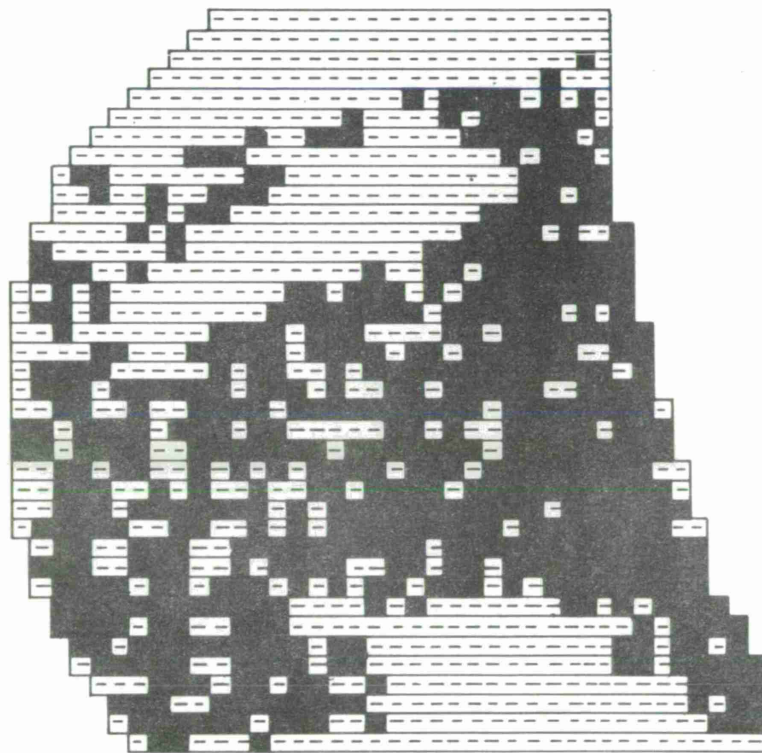
STANDARD PROCESS

49% YIELD
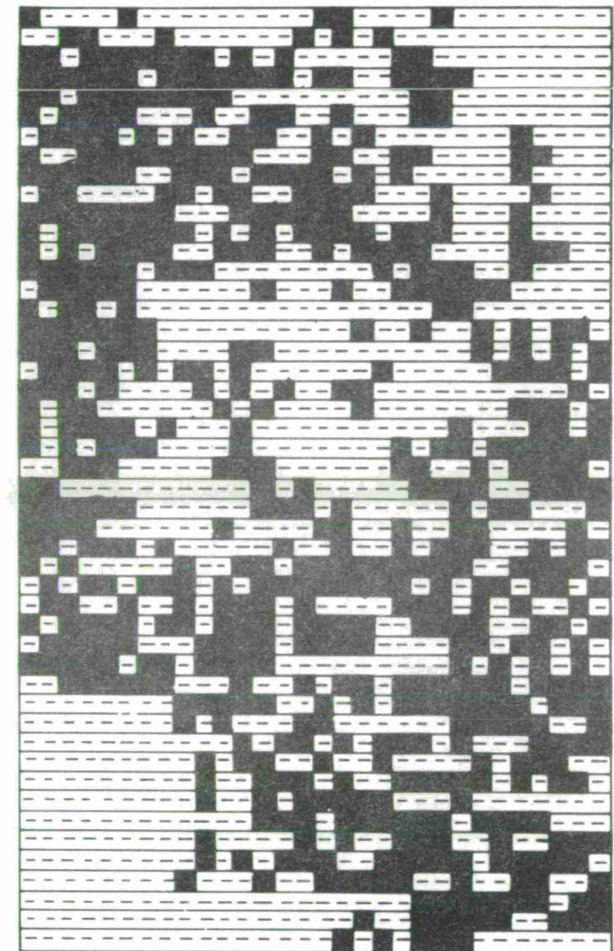
45% YIELD

Figure 19.   Die sort maps of single gates.

yields at least equivalent to the Standard Process when epitaxial

control is improved, and (4) results in gates which are only

one-half as fast as the Standard Process gates. In view of the

speed-power performance goals required for the Processor gates,

the CDI Process does not appear to be applicable to the needs of

this program.

2.6   MULTILEVEL PROCESSING

Early in this program a new set of rules for designing

multilevel metallization structures on small geometry high

performance arrays was generated and documented. The rules

were based primarily upon findings made during the previous

program with Lincoln Laboratory, "Research and Development of

the Technologies Required to Design and Fabricate Ultrahigh-

Speed Computer Systems," wherein previously-used design rules

were evaluated. One of the key changes in the new rules involves

minimum size for vias. The minimum size for vias located over

flat topography is now specified as 0.4 x 0.4 mil; the minimum

size for vias located over topography of any kind, i.e.

underlying metallization, oxide cuts, diffused regions, is now

specified as 0.5 x 0.8 mil^2. (Previously, vias as small as

0.2 mil diameter were used.) These rule changes were made

in order to improve the yield, reproducibility and the reliability

of multilevel metallization structures.[2]

The metallization used in the multilevel structures is evaporated aluminum; the insulating layers are chemical vapor plated phosphosilicate glass. Advantages of this insulator are described in a paper by M. Schlacter et al.[3]

The new design rules for arrays with two levels of interconnections were employed and evaluated on the SMX14 test chip and on the ROM (SMX15) chip. Test results on both of these chips indicated that no problems were encountered with the multilevel structures. Measurements of via resistance, made on a via test pattern on the SMX14 chip, indicated that typical resistance for a via with 0.12 mil^2 cross section was in the range of 65 to 70 mΩ.

During the third interim of this program, a test chip called the "Multilevel Process Chip" (MLPC) was designed. The MLPC was intended for use as a study vehicle, to determine the effectiveness of design rules and process innovations, and as a process monitor, to accompany functional array wafers through the multilevel process. The MLPC contains simulated small geometry microcircuit-level topographies and a number of test patterns designed for testing the quality of the insulating layers and the effectiveness of various geometries of vias and conductors in MSI-LSI structures containing two and three levels of interconnections. Figure 20 is a photomicrograph
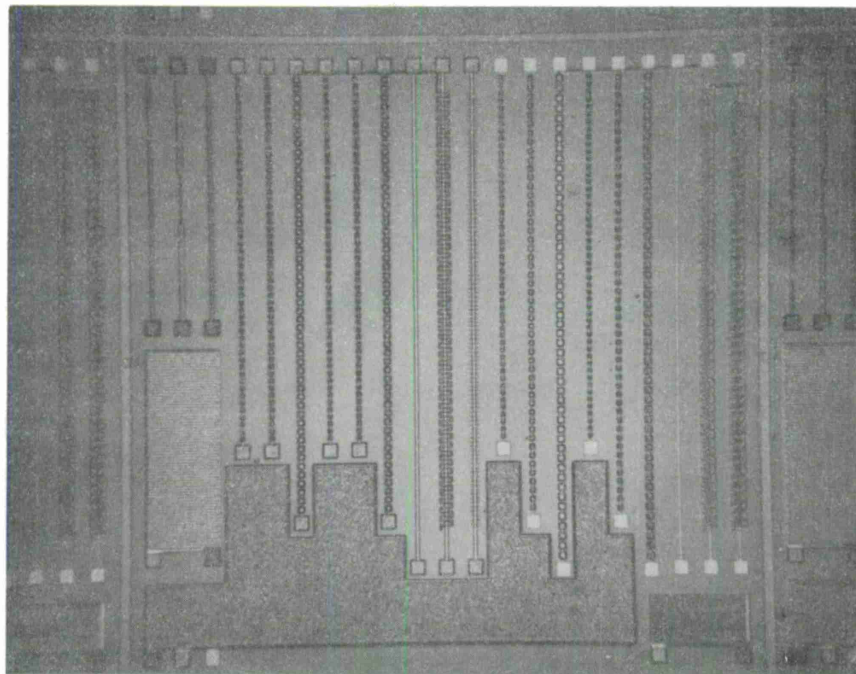
Figure 20. Photomicrograph of Multilevel Process Chip.

of the MLPC. Chip size is 131 x 131 mil^2. Tables V and VI identify

the 21 conduction test patterns, labeled T_1 - T_{21}, and the five

insulator test patterns (capacitor structures), labeled T_A - T_E.

Several groups of MLPC wafers were fabricated for

the purpose of evaluating our multilevel processes and the

usefulness of the MLPC chip. The evaluation netted these

results:

1. Test results verified that our two-level

    metallization design rules and process do

    result in effective multilevel interconnection

    structures. (Film thicknesses in a typical two-

    level structure are: 5500 Å first-level metal;

    7500 Å insulator layer; 12,000 Å top-level

    metal.) With regard to conduction properties

    of the two-level interconnect structures, there

    was no evidence of vias with high or infinite

    resistance. This observation was made while

    sampling as many as 15,000 vias per wafer. The

    sizes of the vias sampled was 0.4 x 0.4 mil^2 and

    0.3 x 0.3 mil^2. Typical values for via resistance

    extrapolated from the via test chains were in

    the range of 20 to 60 mΩ. This is in agreement

    with values for via resistance reported by

TABLE V

LIST OF CONDUCTION TESTS ON MLPC

Test Pattern	Property Being Tested
T_1	Sheet resistance of first-level metal
T_2	Electromigration of first-level metal
T_3	Increase in resistance of a 0.6 mil wide first-level metal stripe due to 100 underlying oxide steps ... typical of isolation channel steps
T_4 T_5 T_6	Resistance through 50 vias, each 0.3 x 0.3 mil^2 ... through first-level insulator ... vias located 0.4 x 0.4 mil^2 0.8 x 0.8 mil^2 over flat topography
T_7 T_8 T_9	Resistance through 50 vias, each 0.3 x 0.3 mil^2 ... through first-level insulator ... vias located 0.4 x 0.4 mil^2 0.8 x 0.8 mil^2 over isolation channel steps
T_{10}	Sheet resistance of second-level metal
T_{11}	Increase in resistance of a 0.6 mil wide second-level metal stripe due to 200 underlying first-level metal steps
T_{12}	Increase in resistance of a 0.6 mil wide second-level metal stripe due to 200 underlying oxide steps typical of isolation channel steps
T_{13} T_{14} T_{15}	Resistance through 50 vias, each 0.4 x 0.4 mil^2 ... through second-level insulator ... vias located 0.8 x 0.8 mil^2 1.0 x 1.0 mil^2 over flat topography
T_{16} T_{17} T_{18}	Resistance through 50 vias, each 0.4 x 0.4 mil^2 ... through second-level insulator ... vias located 0.8 x 0.8 mil^2 1.0 x 1.0 mil^2 over worst case first-level topography, i.e., isolation channels and metallization
T_{19}	Sheet resistance of third-level metal
T_{20}	Increase in resistance of a 0.6 mil wide third-level metal stripe due to 200 underlying second-level metal steps
T_{21}	Increase in resistance of a 0.6 mil wide third-level metal stripe due to 200 underlying second-level metal steps and 100 underlying first-level metal steps.

TABLE VI

LIST OF INSULATOR TESTS ON MLPC

Test Pattern	Property Being Tested
T_a	Pinholes in first-level insulator where it covers "small geometry" topography.
T_b	Pinholes in first-level insulator where it covers edges of first-level metal. Bottom metal electrode pattern has a periphery of 1972 mils and an area of 302 mils^2.
T_c	Pinholes in first-level insulator over planar regions of first-level metal. Bottom electrode area = 2389 mils^2.
T_d	Pinholes in second-level insulator where it covers edges of second level-metal. Bottom metal electrode pattern has a periphery of 100 mils and an area of 50 mils^2.
T_e	Pinholes in second-level insulator over planar regions of second-level metal. Bottom electrode area = 2317 mils^2.

Totta and White,[4] who indicated a resistance spread of 20 to 70 mΩ for 0.5 mil vias in r-f sputtered glass. It was further found that the resistance of second-level metal lines which cross underlying topography is increased only slightly. For example, the increase in resistance of a 100-mil line which is nominally 0.6 mil wide, 11,000 Å thick, and crosses over 200 first-level metal steps is only 10%. This increase is due to some thinning of the top metal as it crosses over the first-level metal stripes. With regard to insulation properties of the deposited insulator, the following values were obtained for lineal pinhole densities, m (i.e., the number of pinholes per unit length in the insulator where it covers the edge of underlying metal), and planar pinhole densities, n (pinholes over planar regions of underlying metal):

$m = 3.3 \times 10^{-5} - 10 \times 10^{-5}$ pinholes per mil

$n = 6.6 \times 10^{-5} - 10 \times 10^{-5}$ pinholes per mil^2

2. The process which we had employed for three-level metal interconnection structures is not completely satisfactory. Electrical opens

were detected in some third-level metal conductor stripes on some wafers. The problem was traced to microcracks in the third-level metal stripes where they cross over the edges of second-level metal stripes. Figure 21 is a photomicrograph of a typical microcrack, taken with a scanning electron microscope. Figure 22 is a 90° cross section showing the microcrack. The phenomenon of formation of these microcracks is believed to be related to that described by Sello[4] for microcracks which form in first-level metal as it crosses over steep angled oxide cuts. Possible ways of avoiding the microcracks include:

a. use of insulator film which more truly reproduces the contour of the under-lying metal;

b. reducing the thickness of underlying metal in order to minimize bulbing of the chemical vapor plated film at the edge of underlying metal;

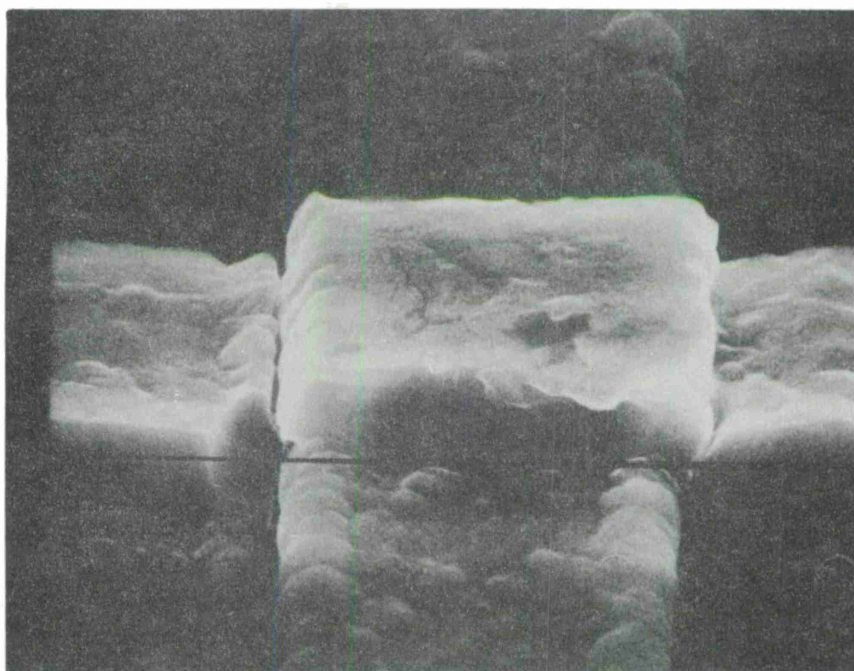c. use of aluminum deposition conditions which avoid microcrack formation;

Figure 21.   Scanning electron microscope photomicrograph
illustrating a microcrack in a third-level
conductor stripe where it crosses over a
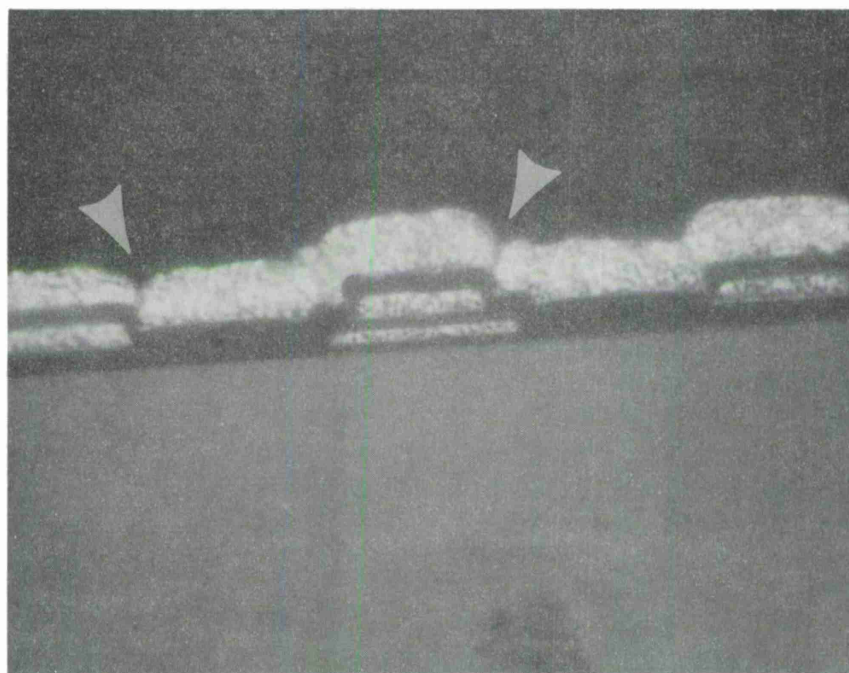second-level conductor stripe.

Figure 22.   90° cross section of a three-level metallization structure wherein microcracks exist in third-level metal conductors where they cross over second-level metal stripes.

> d.   controlled tapering of the edges of
>   underlying metal in order to avoid
>   bulbing of the insulator.
>
> Figure 23 illustrates the merits of controlled
> tapering. All of the above possibilities
> are being examined in order to increase the
> reproducibility and the reliability of the
> three-level metallization process.

2.7 MULTICHIP ASSEMBLY TECHNIQUES

Techniques for multichip assembly of high speed LSI
chips were also investigated during this program. In particular,
the fundamental processes required for solder reflow face-
down bonding and aluminum beam lead technology were established.
The aluminum beam lead technology was developed to a point
where separated beam leaded chips were fabricated. The
vehicle is called the Thermal Test Chip, and Figure 24 shows
a beam leaded Thermal Test Chip.

The choice of multichip interconnection method, which
will be employed with future high speed LSI chips, will have
to be based on factors such as how the yield of assembled
systems will be affected by the assembly method and how power
dissipation in the LSI chips is affected by the assembly
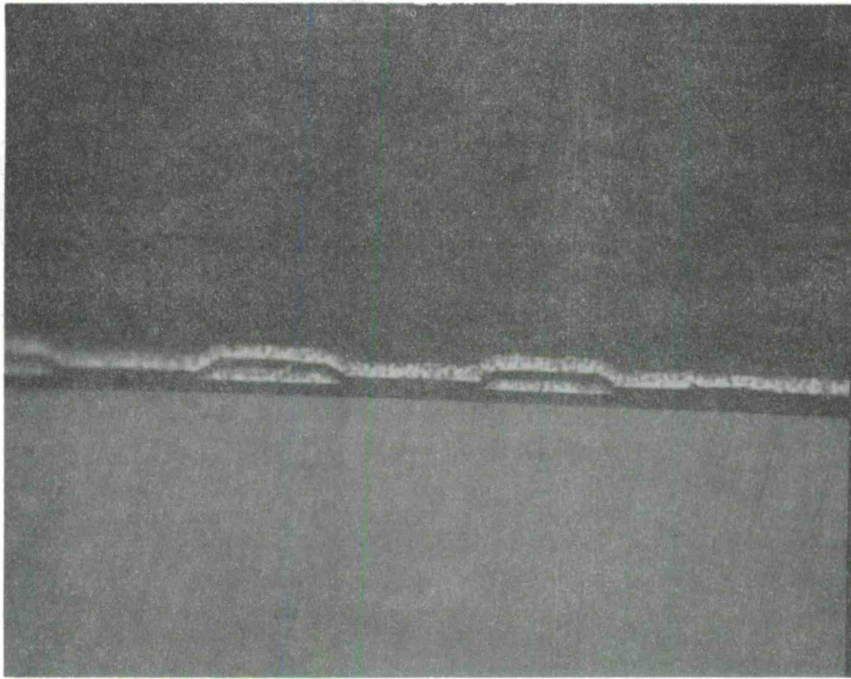method. As a preliminary to evaluating the thermal properties

Figure 23.   90° cross section illustrating how microcracks in top-level conductors can be avoided by tapering the edges of underlying metal conductors.
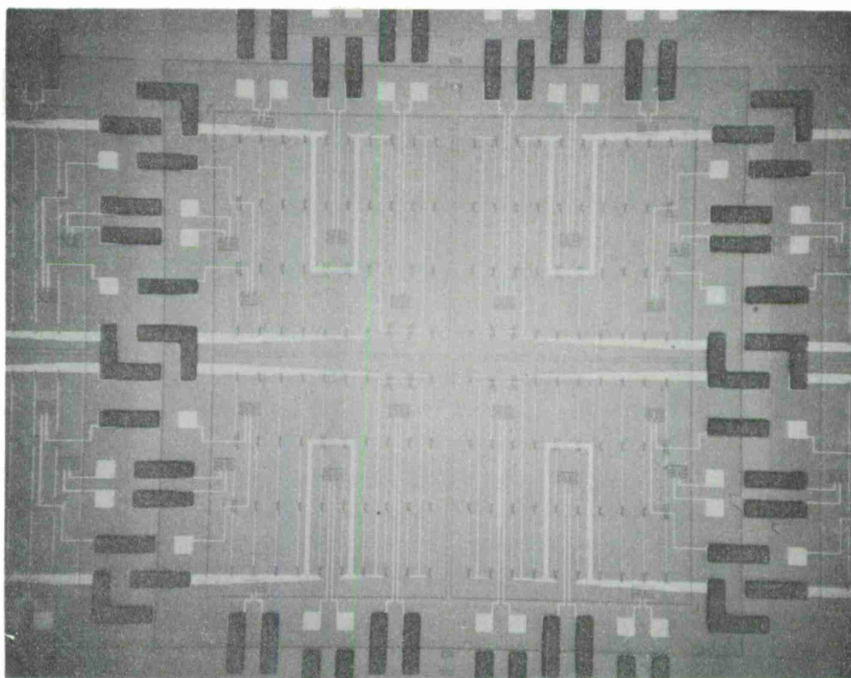
Figure 24.   Photomicrograph of Thermal Test Chip with aluminum
             beam leads.

of multichip assemblies, a study of the thermal properties of large microcircuit chips (typical of anticipated LSI chips of the complexity of the Processor chips), which are conventionally packaged and which dissipate about 1 watt, was made. To accomplish this, a microcircuit test chip referred to as the Thermal Test Chip was designed and fabricated. The Thermal Test Chip is 100 x 100 mils^2 and consists of a matrix of power dissipating resistors and an array of sensing resistors dispersed throughout the chip. All four quadrants of the chip have design symmetry and can be powered independently. Temperature distributions on the chip can be measured using the sensing resistors (after calibrating the sensing resistors as a function of temperature) or through use of infrared scanning techniques.

In one thermal experiment, the entire chip was powered to the 1-watt level and the temperature of the chip surface was sampled in various places. The package was not heat sunk. This experiment was repeated with the package heat sunk to a copper block measuring approximately 1.0" x 0.5" x 0.1". In another experiment, one quadrant of the chip was powered to the 400 mW level. Again junction temperatures were measured with and without heat sinking the package. Tables VII and VIII give results of these experiments. In all experiments, temperature was determined using infrared scanning techniques. The Thermal Test Chips were mounted in 40-lead metal-bottom flat packs having a 0.5" body diameter.

TABLE VII

THERMAL CHARACTERISTICS OF THERMAL TEST CHIP
UNIFORMLY POWERED TO LEVEL OF 1 WATT

	Junction Temperature Range on Chip	Thermal Resistance* - Junction to 27°C Free Air
Package Not Heat Sunk	93.5 - 99.3°C	72.3° C/Watt
Package Heat Sunk to Cu Plate	67.3 - 72.0°C	45.0° C/Watt

* Calculated Using the Maximum Temperature on the Chip

TABLE VIII

THERMAL CHARACTERISTICS OF THERMAL TEST CHIP
WITH ONE QUADRANT POWERED TO 400 mW

	Junction Temperature Range in Powered Quadrant	Junction Temperature Range in Unpowered Quadrants	Thermal Resistance* - Junction to 27°C Free Air
Package Not Heat Sunk	53.7 - 54.5°C	50.7 - 53.5°C	69.0° C/Watt
Package Heat Sunk to Cu Plate	42.3 - 43.4°C	40.7 - 43.4°C	41.2° C/Watt

* Calculated Using the Maximum Temperature on the Chip

These experiments showed that junction temperatures on an LSI chip which dissipates 1 watt and is packaged in a 40-lead, metal-bottom flat pack can be expected to be about 100°C. They further show that simple heat sinking is effective in reducing this temperature. Note that the thermal resistance, junction to air, of the packaged device was similar for the two different power configurations but consistently lower for a single powered quadrant. This is because the factor of increase of the effective thermal resistance through the silicon is less than the factor of decrease in total power when comparing the single-quadrant to the full-chip power configurations. Viewed another way, one can see that thermal interactions between the quadrants (treating each as an integral power source) cause the thermal resistance per quadrant of the system to be higher when all four quadrants are powered.

III - DELIVERIES

During this program the following were delivered to Lincoln Laboratory:

1. Sixty packaged SPX-1 component evaluation chips.

2. Twenty-five package SMX14 gate test chips.

3. Nineteen packaged test transistors from SMX14 chips.

4. Two packaged and programmed ROM's.

5. One wafer of ROM's.

6. Twelve packaged CDI gates.

7. Two CDI gate test chains.

8. Twelve packaged CDI test transistors.

IV - FUTURE WORK

Future work on the extension program proposed would include developing various three-level metal functional arrays from the 80-gate Master Array, i.e. the Loading Test Chip, the 4-bit Full Adder Array, and a 2 x 2 Multiplier Chip.

V - REFERENCES

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13. ABSTRACT

This report describes program progress for the first four interim periods of a research and development program directed toward the development of high density, high performance, complex digital arrays and their application in system feasibility studies of a high speed Central Processor. An important task of this program was to establish subnanosecond-minimum power ECL microcircuit designs which could be used as effective building blocks for the Processor Arrays. This task required the design, fabrication and evaluation of an array test chip containing different microcircuit designs. The task was accomplished; specific small geometry gate and reference bias microcircuits (gate power dissipation was nominally 15 mW, including complementary outputs) were selected and utilized in the design of an 80-gate Processor Master Array Chip. Functioning high speed 256-bit Read Only Memory Arrays were successfully fabricated. A flexible technique for programming these ROM's at the chip level was developed and demonstrated. Yield improvement studies were conducted. This effort included an investigation of the applicability of the CDI process to high speed ECL. It also included the design and evaluation of a complex Multilevel Process Test Chip for characterizing and monitoring multilevel interconnection processes and structures. Techniques for multichip assembly of high speed LSI chips were investigated. In particular, the fundamental processes for solder reflow face-down bonding and aluminum beam lead technology were established. All photomasks employed during the program were designed at MIT Lincoln Laboratory using computer aid.

14. KEY WORDS

Complex digital arrays
Processor Master Array Chip
Read Only Memory Arrays
ROM programming at the chip level
CDI process for high speed ECL

Multilevel interconnection
Face-down bonding
Aluminum beam leads